

**DEVICE  
PERFORMANCE  
SPECIFICATION**

# **KODAK KAC-9638 CMOS IMAGE SENSOR**

**1288 (H) X 1032 (V)  
SXGA 18 fps  
Monochrome CIS**

August 2006  
Revision 1.94

## KAC-9638 Monochrome CMOS Image Sensor SXGA 18 FPS

### General Description

The KAC-9638 is a high performance, low power, 1/2" SXGA CMOS Active Pixel Sensor capable of capturing still, or motion images and converting them to a digital data stream.

Mega-pixel class image quality is achieved by integrating a high performance analog signal processor comprising of a high speed 10 bit A/D converter, fixed pattern noise elimination circuits and a programmable gain amplifier. The offset and black level can be automatically adjusted on chip using a full loop black level compensation circuit.

Furthermore, a programmable smart timing and control circuit allows the user maximum flexibility in adjusting integration time, active window size, gain, frame rate. Various control, timing and power modes are also provided.

### Features

- Video and snapshot operation
- Progressive scan read out with horizontal and vertical flip
- Programmable exposure:
  - Master clock divider
  - Inter row delay
  - Inter frame delay
  - Partial frame integration
- Programmable gain amplifier
- Full automatic servo loop for black level & offset adjustment on each gain channel
- Horizontal & vertical sub-sampling (2:1 & 4:2) with averaging
- Windowing
- Programmable pixel clock, inter-frame and inter-line delays
- I<sup>2</sup>C compatible serial control interface
- Power on reset & power down mode

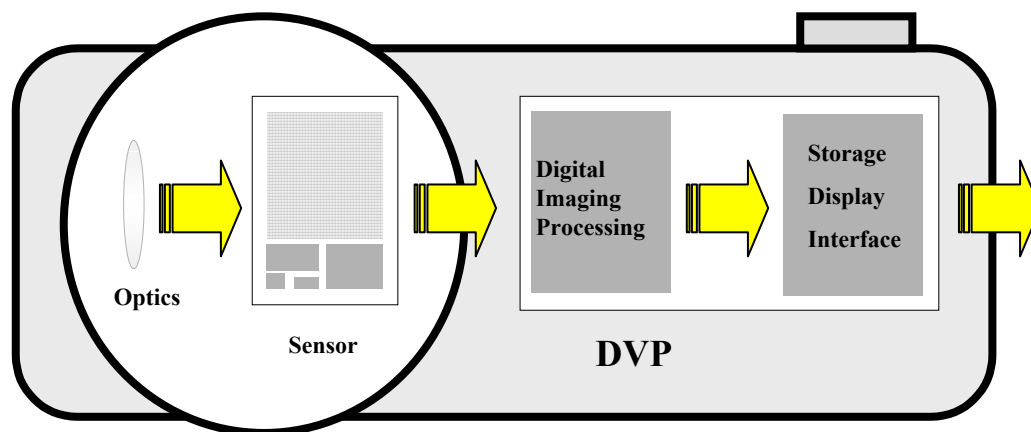
### Applications

- Security Camera
- Machine Vision
- Barcode Scanners
- Biometrics

### Key Specifications

|                      |   |
|----------------------|---|
| Array Format         | Total: 1032 x 1312<br>Active: 1032 (V) x 1288 (H)     |
| Effective Image Area | Total: 6.192mm x 7.872mm<br>Active: 6.192mm x 7.728mm |
| Optical Format       | 1/2"  |
| Pixel Size           | 6.0μm x 6.0μm   |
| Video Outputs        | 8 & 10 Bit Digital                                    |
| Frame Rate           | 18 frames per second                                  |
| Dynamic Range        | 55 dB   |
| Shutter              | Rolling reset   |
| FPN                  | 0.2%  |
| PRNU                 | 1.7%  |
| Sensitivity          | 2.40 V/lux*s  |
| Fill Factor          | 49%   |
| Micro Lens           | none  |
| Package              | 48 LCC  |
| Single Supply        | 3.0V ± 10%  |
| Power Consumption    | 150mW   |
| Operating Temp       | -10°C to 50°C   |

### System Block Diagram



### Overall Chip Block Diagram

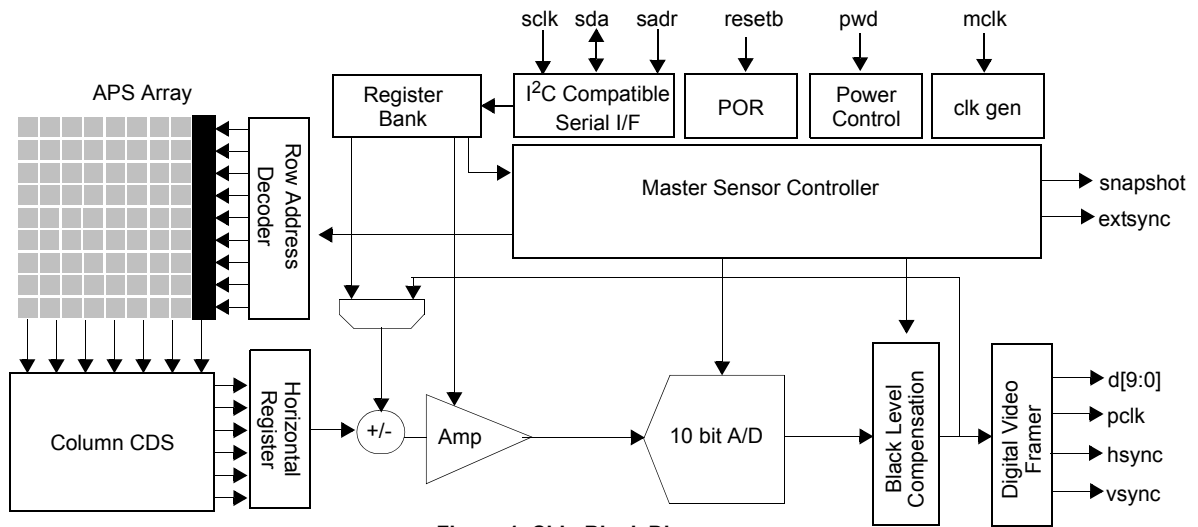


Figure 1. Chip Block Diagram

### Connection Diagram

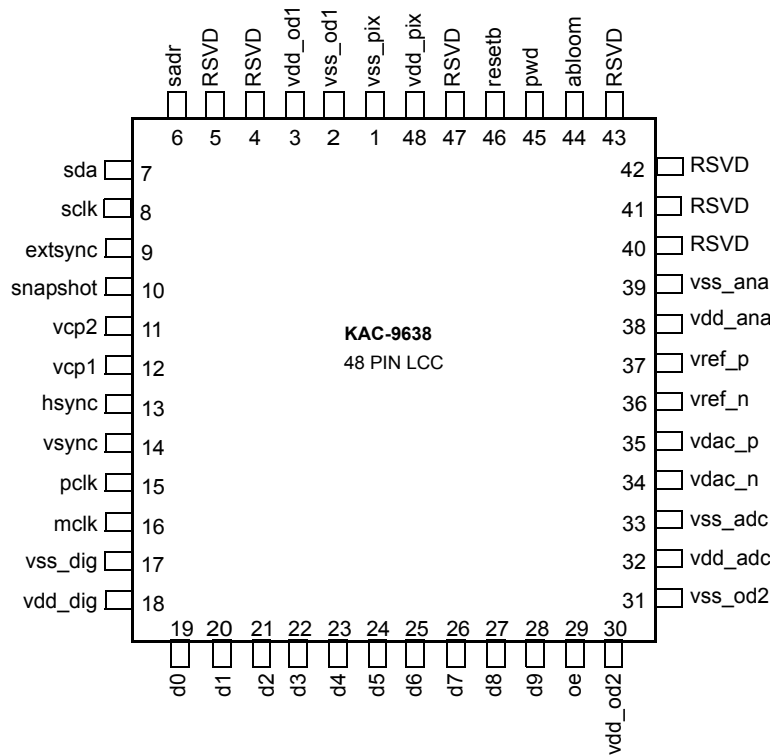


Figure 2. Chip Pin Diagram

### Ordering Information

| Description  | Part Number |
|--|-------------|
| The KAC-9638 is shipped without micro lenses.  | 4H0721      |
| A small PCB that houses the KAC-9638 sensor together with all necessary discrete components. | 3F5383      |
| Lens kit for KAC-9638. Includes 2 M12 1/2" lens.   | 3F5397      |

### Typical Application Circuit

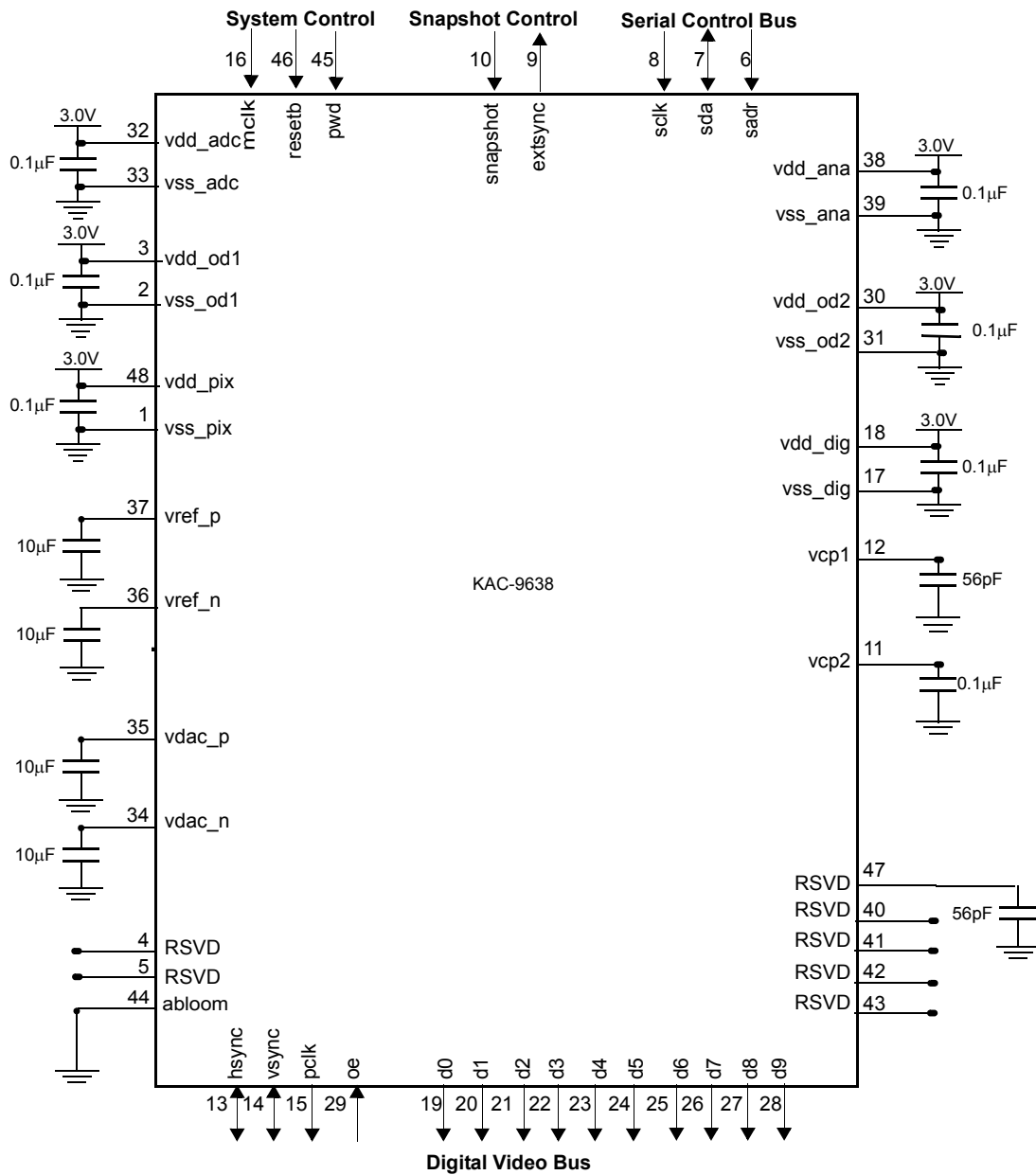


Figure 3. Typical Application Diagram

### Scan Read Out Direction

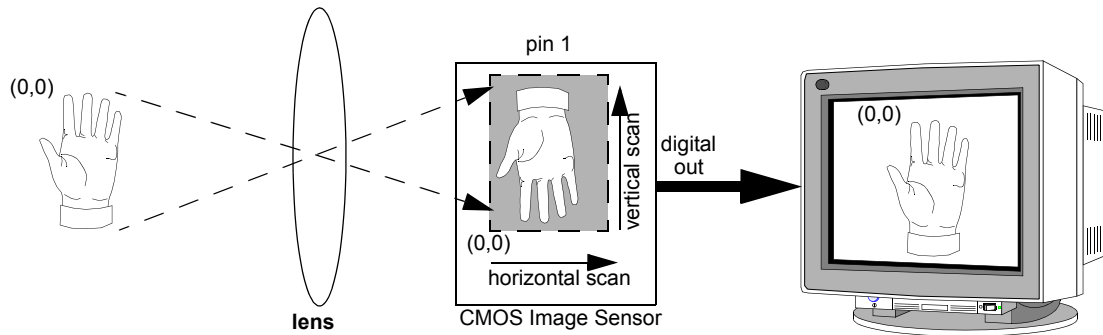


Figure 4. Scan directions and position of origin in imaging system

## Pin Descriptions

| Pin | Name     | I/O | Typ | Description  |
|-----|----------|-----|-----|--|
| 1   | vss_pix  | I   | P   | 0 volt supply for the pixel array  |
| 2   | vss_od1  | I   | P   | 0 volt supply for the digital IO buffers   |
| 3   | vdd_od1  | I   | P   | 3.0 volt supply for the digital IO buffers, connect to <b>vss_od1</b> via a 0.1 $\mu$ f capacitor. .   |
| 4   | RSVD     |     |     | This pin is reserved and should not be connected.  |
| 5   | RSVD     |     |     | This pin is reserved and should not be connected.  |
| 6   | sadr     | I   | D   | Input pin with pull down resistor. This pin is used to program different slave addresses for the sensor in an I <sup>2</sup> C compatible system.  |
| 7   | sda      | IO  | D   | I <sup>2</sup> C compatible serial interface data bus. This is an open drain I/O.  |
| 8   | sclk     | I   | D   | I <sup>2</sup> C compatible serial interface clock. This is an open drain I/O.   |
| 9   | extsync  | O   | D   | The external event synchronization signal is used to synchronize external events in snapshot mode.   |
| 10  | snapshot | I   | D   | Input pin with pull down resistor used to activate (trigger) a snapshot sequence.  |
| 11  | vcp2     | O   | A   | Analog charge pump output, connect to <b>vss_ana</b> via a 0.1 $\mu$ f capacitor. Voltage on this pin should be 5.0 volt.  |
| 12  | vcp1     | O   | A   | Analog charge output, connect to <b>vss_ana</b> via a 56pf capacitor. Voltage on this pin should be <b>vdd_ana</b> +0.3 volt.  |
| 13  | hsync    | IO  | D   | This is a dual mode pin. When the sensor's digital video port is configured to be a master, this pin is an output and is used as the horizontal synchronization pulse. When the sensor's digital video port is configured to be a slave, (the default), this pin is an input and is used as the row trigger. |
| 14  | vsync    | IO  | D   | This is a dual mode pin. When the sensor's digital video port is configured to be a master, this pin is an output and is used as the vertical synchronization pulse. When the sensor's digital video port is configured to be a slave, (the default), this pin is an input and is used as the frame trigger. |
| 15  | pclk     | IO  | D   | Pixel clock.   |
| 16  | mclk     | I   | D   | Sensor's master clock input.   |
| 17  | vss_dig  | I   | P   | 0 volt power supply for the digital circuits.  |
| 18  | vdd_dig  | I   | P   | 3.0 volt power supply for the digital circuits, connect to <b>vss_dig</b> via a 0.1 $\mu$ f capacitor. .   |
| 19  | d0       | O   | D   | Bit 0 of the digital video output bus. This output can be put into tri-stated.   |
| 20  | d1       | O   | D   | Bit 1 of the digital video output bus. This output can be put into tri-stated.   |
| 21  | d2       | O   | D   | Bit 2 of the digital video output bus. This output can be put into tri-stated.   |
| 22  | d3       | O   | D   | Bit 3 of the digital video output bus. This output can be put into tri-stated.   |
| 23  | d4       | O   | D   | Bit 4 of the digital video output bus. This output can be put into tri-stated.   |
| 24  | d5       | O   | D   | Bit 5 of the digital video output bus. This output can be put into tri-stated.   |
| 25  | d6       | O   | D   | Bit 6 of the digital video output bus. This output can be put into tri-stated.   |

## Pin Descriptions (continued)

| Pin | Name    | I/O | Typ | Description   |
|-----|---------|-----|-----|---|
| 26  | d7      | O   | D   | Bit 7 of the digital video output bus. This output can be put into tri-stated.  |
| 27  | d8      | O   | D   | Bit 8 of the digital video output bus. This output can be put into tri-stated.  |
| 28  | d9      | O   | D   | Bit 9 of the digital video output bus. This output can be put into tri-stated.  |
| 29  | oe      | I   | D   | Digital video port output enable with pull up resistor. When this input is driven to a logic zero the digital video port ( <b>d[9:0]</b> , <b>pclk</b> , <b>hsync</b> & <b>vsync</b> ) is tri-stated. |
| 30  | vdd_od2 | I   | P   | 3.0 volt supply for the digital IO buffers, connect to <b>vss_dig</b> via a 0.1 $\mu$ f capacitor. .  |
| 31  | vss_od2 | I   | P   | 0 volt supply for the digital IO buffers.   |
| 32  | vdd_adc | I   | P   | 3.0 volt supply for the 10 bit A/D converter, connect to <b>vss_adc</b> via a 0.1 $\mu$ f capacitor. .  |
| 33  | vss_adc | I   | P   | 0 volt supply for the 10 bit A/D converter.   |
| 34  | vdac_n  | O   | A   | Analog reference output. This pin should be by-passed with a 10 $\mu$ F capacitor.  |
| 35  | vdac_p  | O   | A   | Analog reference output. This pin should be by-passed with a 10 $\mu$ F capacitor.  |
| 36  | vref_n  | O   | A   | Analog reference output. This pin should be by-passed with a 10 $\mu$ F capacitor.  |
| 37  | vref_p  | O   | A   | Analog reference output. This pin should be by-passed with a 10 $\mu$ F capacitor.  |
| 38  | vdd_ana | I   | P   | 3.0 volt supply for analog circuits, connect to <b>vss_ana</b> via a 0.1 $\mu$ f capacitor. .   |
| 39  | vss_ana | I   | P   | 0 volt supply for analog circuits.  |
| 40  | RSVD    |     |     | This pin is reserved and should not be connected.   |
| 41  | RSVD    |     |     | This pin is reserved and should not be connected.   |
| 42  | RSVD    |     |     | This pin is reserved and should not be connected.   |
| 43  | RSVD    |     |     | This pin is reserved and should not be connected.   |
| 44  | abloom  | I   | A   | Anti blooming pin. This pin must be connected to ground.  |
| 45  | pwd     | I   | D   | Input with pull down resistor. When set to a logic 1 the sensor is put into power down mode.  |
| 46  | resetb  | I   | D   | Input with pull up resistor. When set to a logic 0 the sensor is reset to its default power up state.   |
| 47  | RSVD    |     |     | This pin is reserved and should be connected to <b>vss_ana</b> via a 56pf capacitor   |
| 48  | vdd_pix | I   | P   | 3.0 volt supply for the pixel array, connect to <b>vss_ana</b> via a 0.1 $\mu$ f capacitor. .   |

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog).

### Absolute Maximum Ratings (Notes 1 & 2)

|  |                |
|--|----------------|
| Any Positive Supply Voltage                  | 4.2V           |
| Voltage On Any Input or Output Pin           | -0.3V to 4.2V  |
| Input Current at any pin (Note 3)            | ±35mA          |
| Package Input Current (Note 3)               | ±50mA          |
| Package Dissipation at T <sub>A</sub> = 25°C | see Note 4     |
| ESD Susceptibility (Note 5)                  |                |
| Human Body Model                             | 2000V          |
| Machine Model                                | 200V           |
| Peak Soldering Temperature                   | 235°C          |
| Storage Temperature                          | -40°C to 125°C |

### Operating Ratings (Notes 1 & 2)

|                             |                   |
|-----------------------------|-------------------|
| Operating Temperature Range | -10°C ≤ T ≤ +50°C |
| All VDD Supply Voltages     | +2.7V to +3.3V    |

### DC and logic level specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T<sub>MIN</sub> to T<sub>MAX</sub>**; all other limits T<sub>A</sub> = 25°C.

| Symbol  | Parameter                    | Conditions   | Min note 8  | Typical note 7 | Max note 8 | Units    |
|---|------------------------------|--|-------------|----------------|------------|----------|
| <b>sclk, sda, sdr, Digital Input/Output Characteristics</b>                       |                              |  |             |                |            |          |
| V <sub>IH</sub>   | Logical "1" Input Voltage    |  | 0.7*vdd_od  |                | vdd_od+0.5 | V        |
| V <sub>IL</sub>   | Logical "0" Input Voltage    |  | -0.5        |                | 0.3*vdd_od | V        |
| V <sub>OL</sub>   | Logical "0" Output Voltage   | vdd_od = +2.7V, I <sub>out</sub> =3.0mA                |             |                | 0.4        | V        |
| V <sub>hys</sub>  | Hysteresis (SCLK pin only)   | vdd_od > +2.0V   | 0.05*vdd_od |                |            | V        |
| I <sub>leak</sub>   | Input Leakage Current        | V <sub>in</sub> =vdd_od                                |             | 1              |            | µA       |
| <b>mclk, snapshot, pwd, resetb, hsync, vsync Digital Input Characteristics</b>    |                              |  |             |                |            |          |
| V <sub>IH</sub>   | Logical "1" Input Voltage    | vdd_dig = +3.3V  | 2.0         |                |            | V        |
| V <sub>IL</sub>   | Logical "0" Input Voltage    | vdd_dig = +2.7V  |             |                | 0.8        | V        |
| I <sub>IH</sub>   | Logical "1" Input Current    | V <sub>IH</sub> = vdd_dig                              |             | 1              |            | nA       |
| I <sub>IL</sub>   | Logical "0" Input Current    | V <sub>IL</sub> = vss_dig                              |             | -1             |            | nA       |
| <b>d0 - d9, pclk, hsync, vsync, sync, extsync, Digital Output Characteristics</b> |                              |  |             |                |            |          |
| V <sub>OH</sub>   | Logical "1" Output Voltage   | vdd_od=2.7V, I <sub>out</sub> =-1.6mA                  | 2.2         |                |            | V        |
| V <sub>OL</sub>   | Logical "0" Output Voltage   | vdd_od=2.7V, I <sub>out</sub> =-1.6mA                  |             |                | 0.5        | V        |
| I <sub>OZ</sub>   | TRI-STATE Output Current     | V <sub>OUT</sub> = vss_od<br>V <sub>OUT</sub> = vdd_od |             | -0.1<br>0.1    |            | µA<br>µA |
| I <sub>OS</sub>   | Output Short Circuit Current |  |             | +/-17          |            | mA       |
| <b>Power Supply Characteristics</b>   |                              |  |             |                |            |          |
| I <sub>A</sub>  | Analog Supply Current        | Power down mode, no clock<br>Operational mode, @27MHz  |             | 500<br>60      |            | µA<br>mA |
| I <sub>D</sub>  | Digital Supply Current       | Power down mode, no clock<br>Operational mode, @27MHz  |             | 0<br>10        |            | µA<br>mA |

### Power Dissipation Specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T<sub>MIN</sub> to T<sub>MAX</sub>**; all other limits T<sub>A</sub> = 25°C.

| Symbol           | Parameter                 | Conditions        | Min note 8 | Typical note 7 | Max note 8 | Units    |
|------------------|---------------------------|-------------------|------------|----------------|------------|----------|
| P <sub>dwn</sub> | Power Down                |                   |            | 2.0            |            | mW       |
| PWR              | Average Power Dissipation | @27 MHz<br>@12MHz |            | 210<br>150     |            | mW<br>mW |

## Video Amplifier Specifications

The following specifications apply for all VDD pins= +3.0V. **Boldface limits apply for TA = T<sub>MIN</sub> to T<sub>MAX</sub>**; all other limits TA = 25°C

| Symbol | Parameter       | Conditions          | Min (note 8) | Typical (note 7) | Max (note 8) | Units |
|--------|-----------------|---------------------|--------------|------------------|--------------|-------|
|        | Gain Resolution |                     |              | 7                |              | Bits  |
|        | Step Size       | (Gain / Resolution) |              | 0.125            |              | dB    |
|        | Maximum Gain    | Low light bit off   |              | 16               |              | dB    |
|        | Minimum Gain    | Low Light bit off   |              | 0.0              |              | dB    |

## AC Electrical Characteristics

The following specifications apply for All VDD pins = +3.0V. **Boldface limits apply for TA = T<sub>MIN</sub> to T<sub>MAX</sub>**; all other limits TA = 25°C.

| Symbol                            | Parameter                       | Conditions           | Min note 8 | Typical note 7 | Max note 8 | Units   |
|-----------------------------------|---------------------------------|----------------------|------------|----------------|------------|---------|
| F <sub>mclk</sub>                 | Input Clock Frequency           |                      | 12         |                | 27         | MHz     |
| T <sub>ch</sub>                   | Clock High Time                 | @ CLK <sub>max</sub> | 16.0       |                |            | ns      |
| T <sub>cl</sub>                   | Clock Low Time                  | @ CLK <sub>max</sub> | 16.0       |                |            | ns      |
|                                   | Clock Duty Cycle                | @ CLK <sub>max</sub> | 45/55      | 50/50          | 55/45      | min/max |
| T <sub>rc</sub> , T <sub>fc</sub> | Clock Input Rise and Fall Time  |                      |            | 3              |            | ns      |
| F <sub>hclk</sub>                 | Internal System Clock Frequency |                      | 12         |                | 27         | MHz     |
| T <sub>reset</sub>                | Reset pulse width               |                      | 1.0        |                |            | μs      |

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: All voltages are measured with respect to **vss\_dig = vss\_ana = vss\_adc = vss\_od1 = vss\_od2 = 0V**, unless otherwise specified.
- Note 3: When the voltage at any pin exceeds the power supplies (VIN < [vss\_dig or vss\_ana or vss\_adc or vss\_od1 or vss\_od2] or VIN > [vdd\_dig or vdd\_ana or vdd\_adc or vdd\_od1 or vdd\_od2]), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.
- Note 4: The absolute maximum junction temperature (TJmax) for this device is 150°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (θJA), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJmax - TA)/θJA. In the 48-pin LCC, θJA is 69°C/W, so PDMAX = 1,811mW at 25°C and 1,449 mW at the maximum operating ambient temperature of 50°C. Note that the power dissipation of this device under normal operation will typically be about 215 mW. The values for maximum power dissipation listed above will be reached only when the KAC-9638 is operated in a severe fault condition.
- Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.
- Note 6: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above AV+ and below AGND.
- Note 7: Typical figures are at TJ = 25°C, and represent most likely parametric norms
- Note 8: Test limits are guaranteed to AOQL (Average Outgoing Quality Level).



## CMOS Active Pixel Array Specifications

| Parameter                      | Value             | Units  |
|--------------------------------|-------------------|--------|
| Number of pixels (row, column) |                   |        |
| Total                          | 1032 x 1312       | pixels |
| Active                         | 1032 x 1288       | pixels |
| Array size (x,y Dimensions)    |                   |        |
| Total                          | 6.192mm x 7.872mm | mm     |
| Active                         | 6.192mm x 7.728mm | mm     |
| Pixel Pitch                    | 6.0               | μ      |
| Fill Factor without micro-lens | 49                | %      |

## Image Sensor Specifications

The following specifications apply for All VDD pins = +3.3V, T<sub>A</sub> = 25°C, Illumination Color Temperature = 2500°K, IR cutoff filter at 700nm, mclk = 27MHz, frame rate = 15Hz, unity video gain.

| Parameter                        | Description   | Min note 8 | Typical note 7 | Max note 8 | Units   |
|----------------------------------|---|------------|----------------|------------|---------|
| Optical Sensitivity <sup>1</sup> | Measured at the input of the A/D  |            | 2.40           |            | V/lux*s |
| Dark Signal                      | The pixel output signal due to dark current.  |            | 0.15           |            | V/s     |
| Read Noise                       | The RMS temporal noise of the pixel output signal in the dark averaged over all pixels in the array.                        |            | 1.5            |            | LSBs    |
| Dynamic Range                    | The ratio of the saturation pixel output signal and the read noise expressed in dB.   |            | 55             |            | dB      |
| FPN                              | Fixed Pattern Noise: the RMS spatial noise in the dark excluding the effect of read noise.                                  |            | 0.2            |            | %       |
| PRNU                             | Photo Response Non Uniformity: the RMS variation of pixel sensitivities as a percentage of the average optical sensitivity. |            | 1.5            |            | %       |

<sup>1</sup> The optical sensitivity at the A/D output, in units of LSBs/lux\*s, can be calculated using:  $\frac{1024}{v_{refp}-v_{refn}}$  · Optical Sensitivity

## Blemish Specifications

Due to random process deviations, not all pixels in an image sensor array will react in the same way to a given light condition. These variations are known as blemishes.

Eastman Kodak tests the KAC-9638 CMOS image sensor under both dark and illuminated conditions. These two tests are referred to as “Dark Tests” and “Standard Light Tests” respectively.

For full documentation of the KAC-9638 blemish specification and test conditions please refer to the “KAC-9638 Blemish Specification” document.

Sensor Response Curves

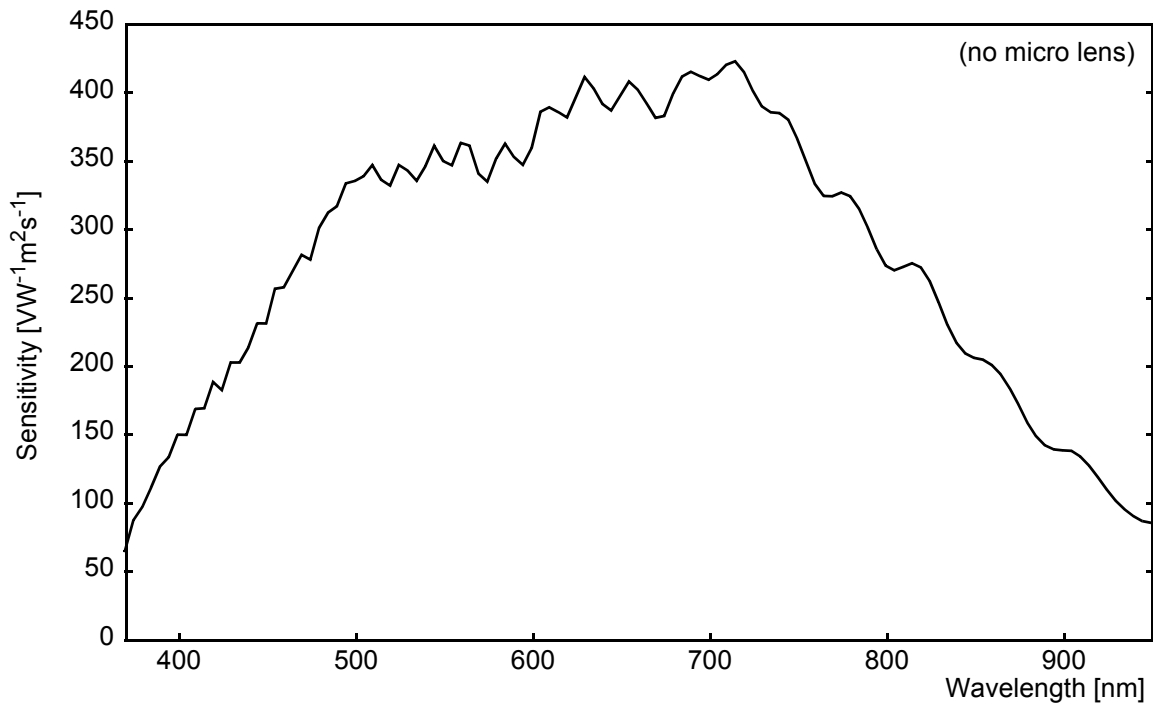
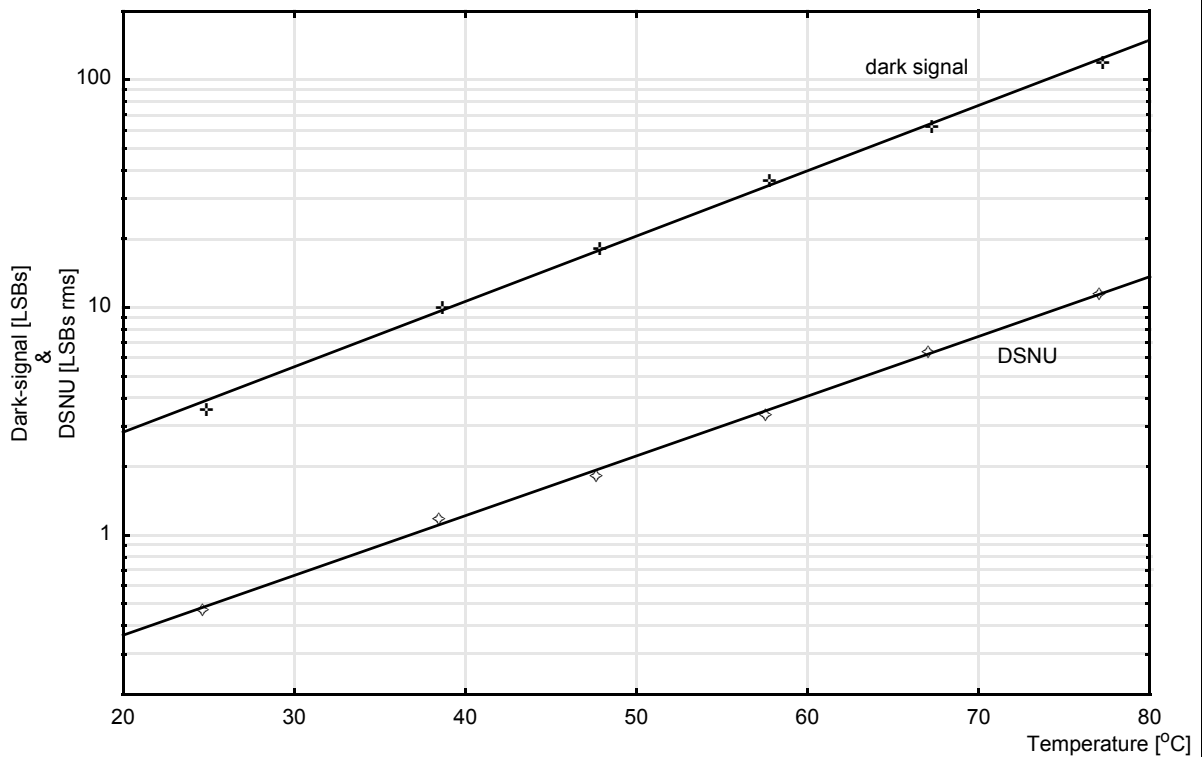


Figure 5. Spectral Response Curve



Notes:

- 1) The dark signal and DSNU both increase linearly with integration time. The results in the graph were measured at 33 ms integration time and unity gain.
- 2) At any temperature, the total spatial noise in the dark can be found by quadratically adding the offset FPN from the 'Image Sensor Specifications' table and the DSNU from this graph.

Figure 6. Dark signal and Dark Signal Non-Uniformity versus Temperature

# Functional Description

## 1.0 OVERVIEW

### 1.1 Light Capture and Conversion

The KAC-9638 contains a CMOS active pixel array consisting of 1032 rows by 1288 columns. 24 columns of optically shielded (black) pixels are provided to the right of the array as shown in Figure 7.

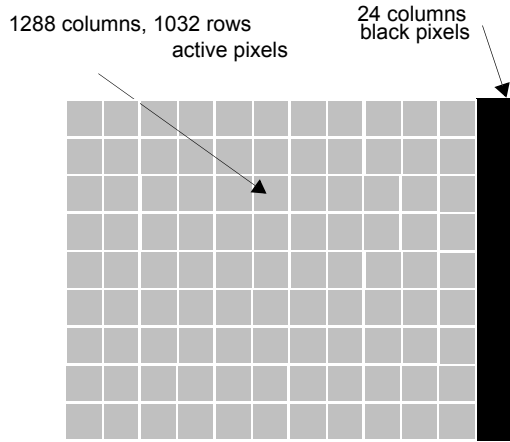


Figure 7. CMOS APS region of the KAC-9638

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array one row at a time as shown in Figure 8. Note that all pixels in the same row are simultaneously reset, but not all pixels in the array.

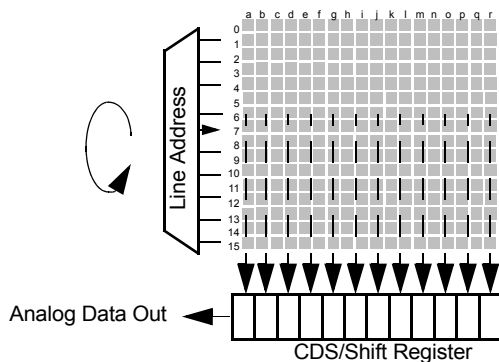


Figure 8. CMOS APS Row and Column addressing scheme

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in Figure 8.

Once the correlated double sampled signals have been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time.

The analog pixel signal is then fed into an analog gain channel as shown in figure 9. The gain channel can be digitally programmed allowing the signal level of pixel to be adjusted.

After gain adjustment the analog value of each pixel is converted to a 10 bit digital data as shown in figure 9.

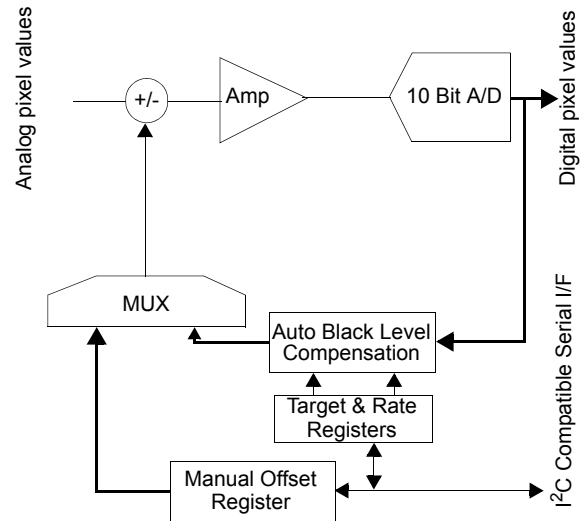


Figure 9. Analog Signal Conditioning & Conversion to Digital

The black level together with the full analog signal path offset is automatically compensated as shown in figure 9. This can be manually overridden.

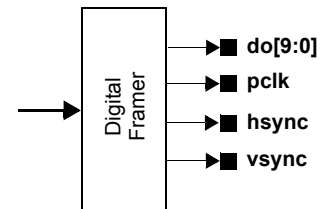


Figure 10. Digital Pixel Processing.

Finally the pixel data is framed and output on the digital video bus as shown in figure 10.

### 1.2 Program and Control Interfaces

The programming, control and status monitoring of the KAC-9638 is achieved through a two wire I<sup>2</sup>C compatible serial bus. A device address pin is provided allowing two different device addresses to be selected for the serial interface as shown in Figure 11.

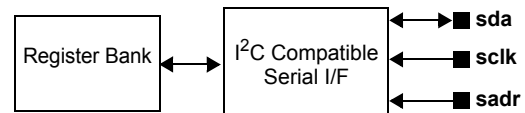


Figure 11. Control Interface to the KAC-9638.

Snapshot control and status pins are provided to facilitate single frame capture (see Figure 12).

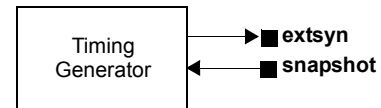


Figure 12. Snapshot & External Event Trigger Signals

## Functional Description (continued)

### 2.0 DOUBLE BUFFERED REGISTERS

All programmable registers that effect the frame rate and integration timing are double buffered; such that the new values only take effect at the start of the new frame. When writing to all split double buffered registers, e.g. ITIMEH and ITIMEL, the following procedure must be followed:

- to change both the MSB and LSB, first write to the MSB register and then write to the LSB register,
- to change only the MSB, first write to the MSB register and then write the unchanged value of the LSB to the LSB register,
- to only change the LSB write to the LSB register.

### 3.0 WINDOWING

The integrated timing and control circuit allows any size window in any position within the active region of the array to be read out with a 4x4 pixel resolution. The window read out is called the "Active Window".

Four coordinates (start row and column addresses, end row and column addresses) need to be programmed to define the size and location of the "Active Window" to be read out (see Figure 13).

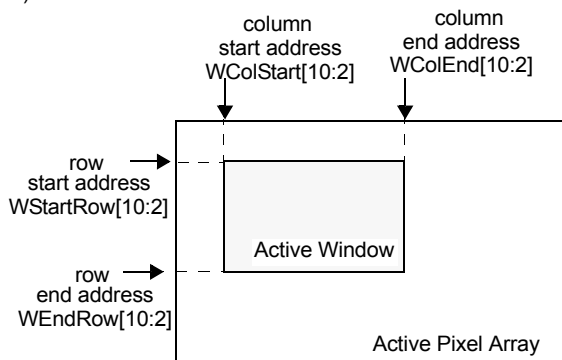


Figure 13. Windowing

**Notes:**

- By default the "Active Window" is an optically centered with a size of 1280 columns by 1024 rows as shown in figure 14.
- The "Active Window" registers are double buffered.

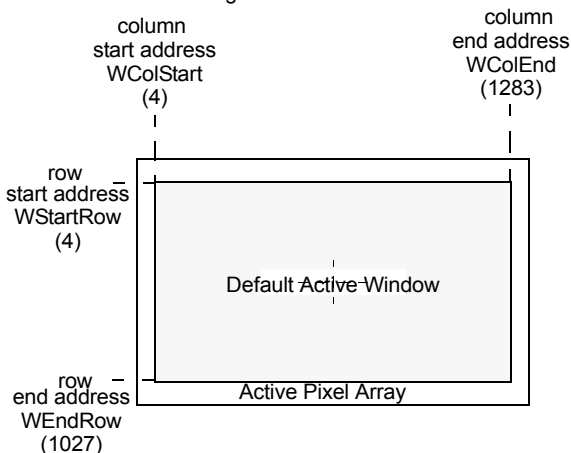


Figure 14. Default Active Window

### 4.0 ARRAY READOUT

The pixels in the array are read out in progressive scan. In progressive scan, every pixel in every row in the defined "Active Window" is consecutively read out, one pixel at a time. The first 8 pixels of every row are black (regardless of scan direction) unless masked out by setting the *BlkPixelEn* bit (bit 6) of the DVBUSCONFIG2 register (register 0x54h) to a logic 0.

The scan direction can be programmed as follows:

| Scan Direction                                 | VScanDir | HScanDir |
|--|----------|----------|
| Default Scan Direction                         | 1        | 1        |
| Reverse Vertical Scan Direction                | 0        | 1        |
| Reverse Horizontal Scan Direction              | 1        | 0        |
| Reverse Vertical and Horizontal Scan Direction | 0        | 0        |

#### 4.1 Default Scan Direction

The default scan direction is to consecutively read out, one pixel at a time, starting with the left most pixel in the top most row. Hence, for the example shown in Figure 15, the read out order will be *a0, b0, ..., r0* then *a1, b1, ..., r1* and so on until pixel *r10* is read out. See figure 15.

#### 4.2 Reverse Vertical Scan Direction

The vertical scan direction can be reversed by setting the "VScanDir" bit in the VSCAN register to a logic 0, while setting the HScanDir bit in the HSCAN register to a logic 1. In this case for the example shown in Figure 15, the read out order will be *a10, b10, ..., r10* then *a9, b9, ..., r9* and so on until pixel *r0* is read out.

#### 4.3 Reverse Horizontal Scan Direction

The horizontal scan direction can be reversed by setting the "HScanDir" bit in the HSCAN register to a logic 0, while setting the "VScanDir" bit in the VSCAN register to a logic 1. In this case for the example shown in Figure 15, the read out order will be *r0, q0, ..., a0* then *r1, q1, ..., a1* and so on until pixel *a10* is read out.

#### 4.4 Reversing The Horizontal & Vertical Scan Direction

The horizontal scan direction can be reversed by setting both the "HScanDir" bit in the HSCAN and the "VScanDir" bit in the VSCAN register to a logic 0. In this case for the example shown in Figure 15, the read out order will be *r10, q10, ..., a10* then *r9, q9, ..., a9* and so on until pixel *a0* is read out.

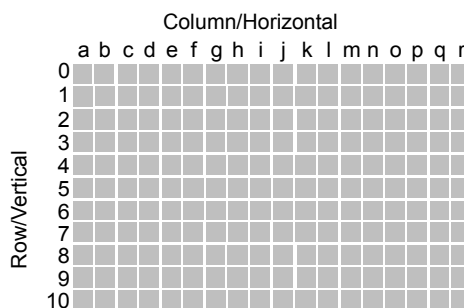


Figure 15. Progressive Scan Read Out Mode

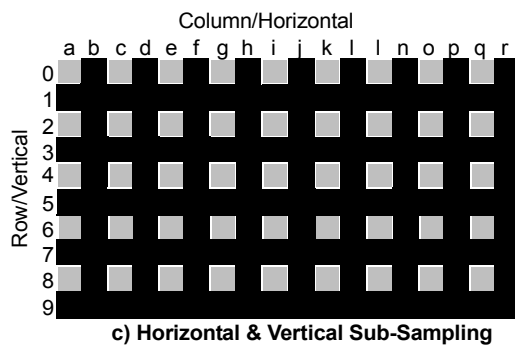
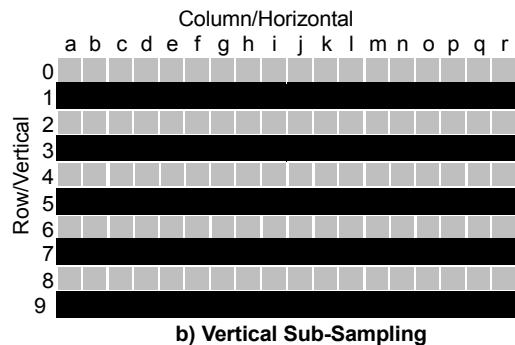
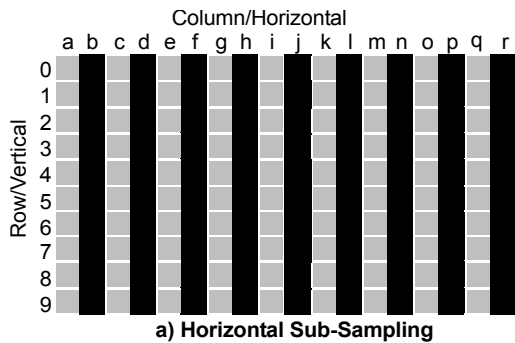
## Functional Description (continued)

### 5.0 SUB-SAMPLING MODES

#### 5.1 2:1 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the “Active Window” vertically, horizontally or both, with an aspect ratio of 2:1 as illustrated in figure 16.

| Register Bit | VIDCONFIG Color | VSCAN VSub | HSCAN HSub |
|--------------|-----------------|------------|------------|
| Vertical     | 0               | 1          | 0          |
| Horizontal   | 0               | 0          | 1          |
| Both         | 0               | 1          | 1          |



■ Read Out                      ■ Not Read Out

Figure 16. Example of 2:1 Sub-sampling

- Note a: The pixel read out will depend on the programmed scan order as described in section 4.0.  
 Note b: For max FPN performance it is recommended to always switch on the averaging feature when sub-sampling (see next section).

#### 5.2 2:1 Sub-Sampling with Averaging

The timing and control circuit can be programmed to average neighboring pixels in the analog domain before sub-sampling. This can be done in the horizontal and vertical direction shown in the table below

| Register Bit | VIDCONFIG Color | VSCAN VAvr | HSCAN HAvr |
|--------------|-----------------|------------|------------|
| Vertical     | 0               | 1          | 0          |
| Horizontal   | 0               | 0          | 1          |
| Both         | 0               | 1          | 1          |

When **vertical** 2:1 sub-sampling with averaging is selected, neighboring pixels in the vertical direction are combined as shown in figure 17. The value of the combined pixel is given by:

$$\frac{V_1 + V_2}{2}$$

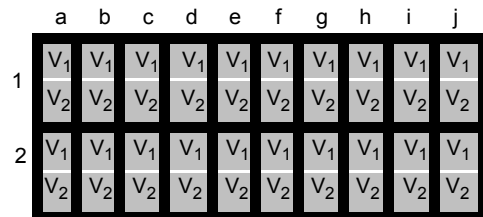


Figure 17. :2:1 Vertical Sub-Sampling with Averaging

When **horizontal** 2:1 sub-sampling with averaging is selected, neighboring pixels in the horizontal direction are combined as shown in figure 18. The value of the combined pixel is given by

$$H_1 + H_2$$

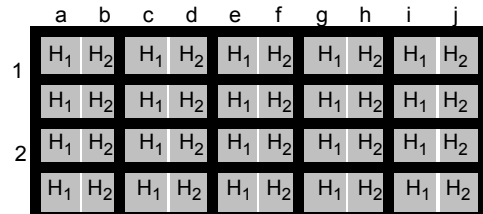


Figure 18. 2:1 Horizontal Sub-Sampling with Averaging

When **both**, horizontal & vertical 2:1 sub-sampling with averaging is selected, neighboring pixels in both directions are combined as shown in figure 19. The value of the combined pixel is given by

$$\frac{H_1 + H_2 + V_1 + V_2}{2}$$

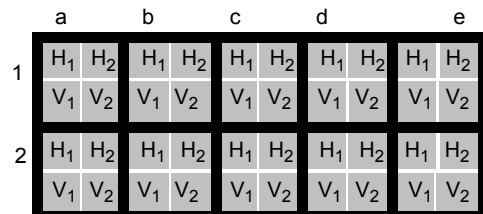


Figure 19. 2:1 Both Subsampling with Averaging

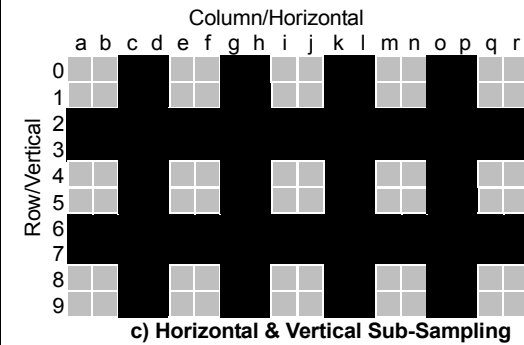
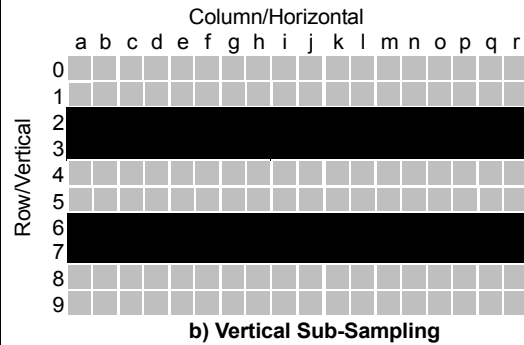
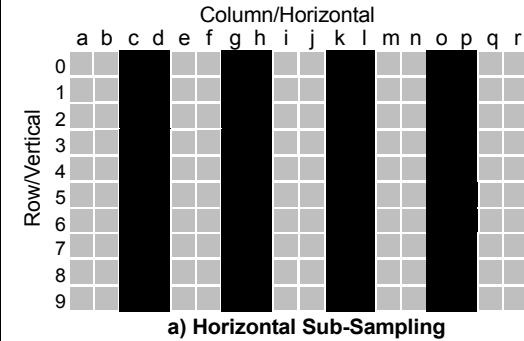
Note that the pixel read out will depend on the programmed scan order as described in section 4.0.

## Functional Description (continued)

### 5.3 4:2 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 4:2 as illustrated in figure 20

| Register Bit | VIDCONFIG<br><i>Color</i> | VSCAN<br><i>VSub</i> | HSCAN<br><i>HSub</i> |
|--------------|---------------------------|----------------------|----------------------|
| Vertical     | 1                         | 1                    | 0                    |
| Horizontal   | 1                         | 0                    | 1                    |
| Both         | 1                         | 1                    | 1                    |



■ Read Out      ■ Not Read Out

Figure 20. Example 4:2 Sub-sampling

- Note a: The pixel read out will depend on the programmed scan order as described in section 4.0.
- Note b: For max FPN performance it is recommended to always switch on the averaging feature when sub-sampling (see next section).

### 5.4 4:2 Sub-Sampling with Averaging

The timing and control circuit can be programmed to average neighboring pixels in the analog domain before sub-sampling. This can be done in the horizontal and vertical direction as shown in the table below:

| Register Bit | VIDCONFIG<br><i>Color</i> | VSCAN<br><i>VAvr</i> | HSCAN<br><i>HAvr</i> |
|--------------|---------------------------|----------------------|----------------------|
| Vertical     | 1                         | 1                    | 0                    |
| Horizontal   | 1                         | 0                    | 1                    |
| Both         | 1                         | 1                    | 1                    |

When **vertical** 4:2 sub-sampling with averaging is selected, neighboring pixels in the vertical direction are combined as shown in figure 21. The value of the combined pixel is given by:

$$\frac{V_1 + V_2}{2}$$

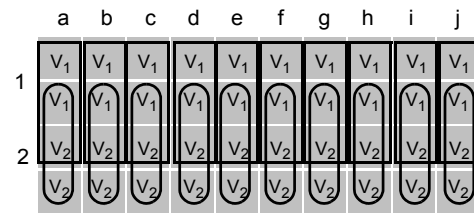


Figure 21. :4:2 Vertical Sub-Sampling with Averaging

When **horizontal** 4:2 sub-sampling with averaging is selected, neighboring pixels of the same color in the horizontal direction are combined as shown in figure 22. The value of the combined pixel is given by

$$H_1 + H_2$$

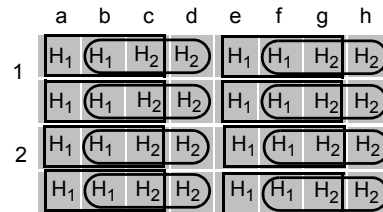


Figure 22. 4:2Horizontal Sub-sampling with Averaging

When **both**, horizontal & vertical 4:2 sub-sampling with averaging is selected, neighboring pixels of the same color in both directions are combined as shown in figure 23. The value of the combined pixel is given by

$$\frac{H_1 + H_2 + V_1 + V_2}{2}$$

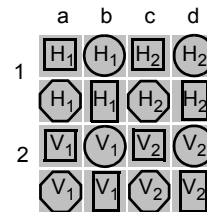


Figure 23. 4:2 Both Sub-sampling with Averaging

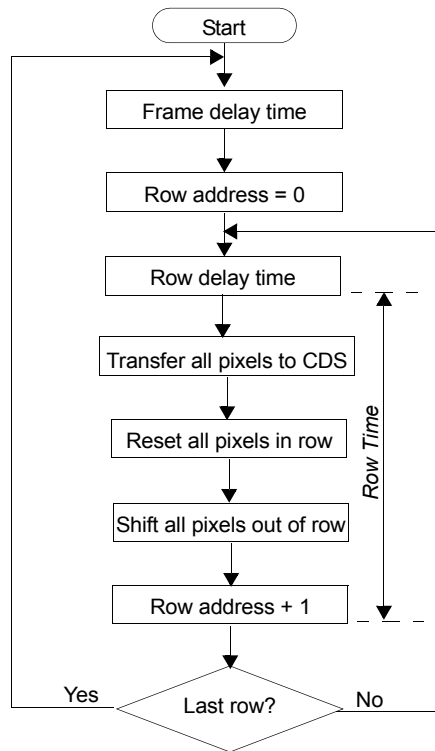
Note that the pixel read out will depend on the programmed scan order as described in section 4.0.

## Functional Description (continued)

### 6.0 FRAME RATE & EXPOSURE CONTROL

#### 6.1 Introduction

The frame time is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and present it on the digital video port. This is not a concurrent process and is characterized in a series of events each requiring a certain amount of time as shown in Figure 24.



**Figure 24. Frame Readout Flow Diagram**

The following factors affect frame rate, exposure and signal level, the:

- frequency of *Hclk*
- size of the "Active Window"
- subsampling mode
- programmed row delay
- programmed frame delay.

The following factor effects signal level only.

- analog gain

The following factor effects exposure & signal level:

- programmed partial frame integration time

This section describes how to program the frame rate and exposure time.

#### 6.2 Analog Gain

A programmable analog gain amplifier is provided, allowing the gain level of the in-coming pixels to be adjusted before the analog to digital conversion.

16dB of gain programmable in 128 steps of 0.125dB, (see the PGA register). See Figure 25 for graph of linear gain factor vs. pga register setting. Note: Set register 0x4Ah to 0x00h when using monochrome sensor.

A further 5.6dB of gain can be added by setting the *LowLight* bit in the OPCTL register to a logic 1.

### Functional Description (continued)

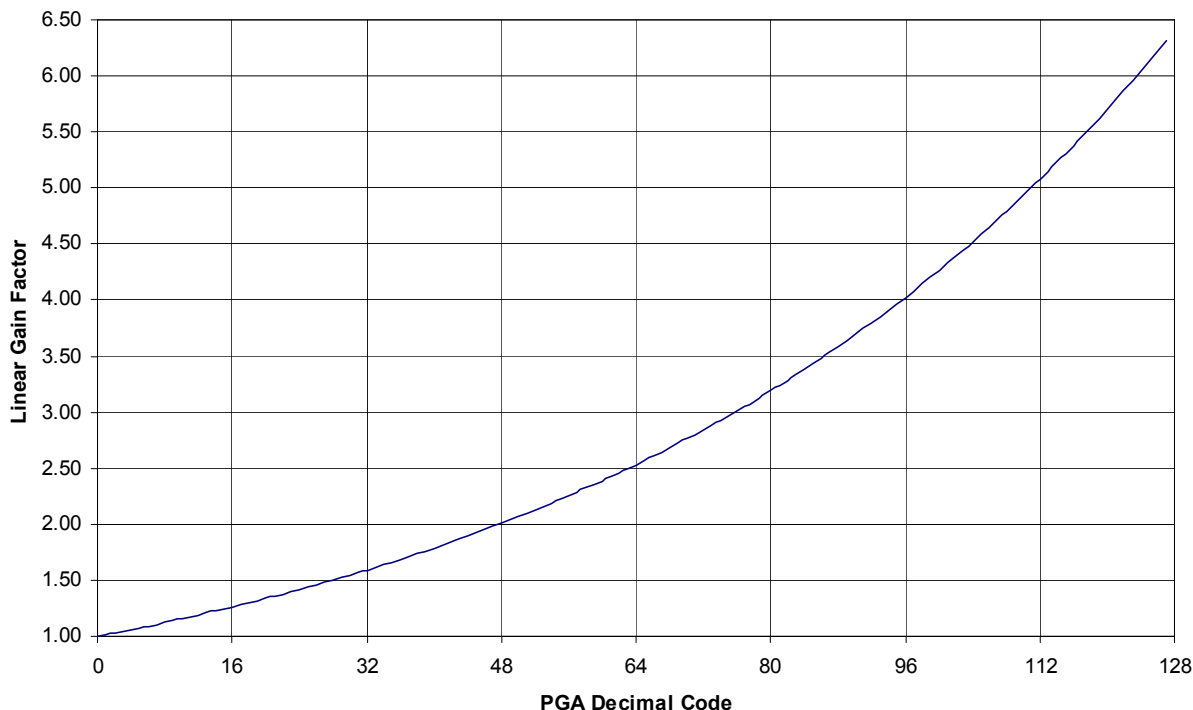


Figure 25. Gain Plot with low light bit off

#### 6.3 Clock Generation

The KAC-9638 contains a clock generation module (figure 26) that will create three clocks as follows:

**Hclk**, the horizontal clock. This is an internal system clock and can be programmed to be the input clock (**mclk**) or **mclk** divided by 1 or 2. All exposure times are in multiples of this clock.

To set the frequency of this clock the *HclkGen* bits in the VCLKGEN register should be programmed.

**pclk** the pixel clock. This is the external pixel clock that appears at the digital video port. By default **pclk** is free running and its frequency is always equal to *Hclk* (see figure 26).

**pclk** can be programmed to the following modes:

- Data Ready Mode, where **pclk** clock will go active every time a valid pixel appears on the data out bus by setting the *PixClkMode* bit of the DVBUSCONFIG1 to a logic 1.
- Reverse Polarity Mode, where the polarity of **pclk** is negated by programming the *PixClkPol* bit in the DVBUSCONFIG2 register.

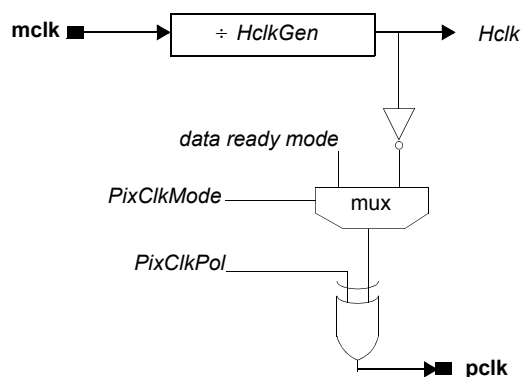


Figure 26. Clock Generation Module



## Functional Description (continued)

### 6.4 Full Frame Integration

Full frame integration is when each pixel in the array integrates light incident on it for the duration of a frame (see Figure 27).

The number of pixels processed per row is given by:

$$N_{pix} = (W_{EndCol} - W_{StartCol} + 1) * M_{Hfactor}$$

Where:

$W_{EndCol}$

is the "Active Window" column end address as programmed in registers WCOLE and WCOLLSB.

$W_{StartCol}$

is the "Active Window" column start address as programmed in registers WCOLS and WCOLLSB.

$M_{Hfactor}$

Is 1 when horizontal subsampling is disabled and 0.5 when horizontal subsampling is enabled.

The number of  $Hclk$  clock cycles required to process & shift out one row of pixels is given by:

$$RN_{Hclk} = R_{opcycle} + R_{itime} + N_{pix} + R_{delay}$$

Where:

$R_{opcycle}$

is a fixed integer value of 140 representing the Row Operation Cycle Time in multiples of  $Hclk$  clock cycles. It is the time required to carry out all fixed row operations outlined in Figure 24.

$R_{itime}$

When partial frame integration is enabled, (PrtFrmEn bit in the ITIMECONFIG register is set to a logic 1),  $R_{itime}$  is a fixed integer of 34. When Partial frame integration is disabled, (PrtFrmEn bit in the ITIMECONFIG register is set to a logic 0),  $R_{itime}$  is 0.

$N_{pix}$

Is the number of pixels processed in a row.

$R_{delay}$

a programmable value between 0 & 8191 representing the Row Delay Time in multiples of  $Hclk$ . This parameter allows the Row Operation Cycle time to be extended. The  $R_{delay}$  value is programmed in the RDELAYH and RDELAYL registers.

The number of rows in the active window is given by:

$$N_{rows} = (W_{EndRow} - W_{StartRow} + 1) * M_{Vfactor}$$

Where:

$W_{EndRow}$

is the "Active Window" row start address as programmed in registers WROWE and WROWLSB.

$W_{StartRow}$

is the "Active Window" row start address as programmed in registers WROWS and WROWLSB.

$M_{Vfactor}$

Is 1 when vertical subsampling is disabled and 0.5 when vertical subsampling is enabled.

The number of  $Hclk$  clocks required to process a full frame is given by:

$$FN_{Hclk} = [N_{rows} + F_{delay}] * RN_{Hclk}$$

Where:

$N_{rows}$

is the number of rows in the "Active Window".

$F_{delay}$

a programmable value between 0 & 32767 representing the Inter Frame Delay in multiples of  $RN_{Hclk}$ . This parameter allows the frame time to be extended. (See the Frame Delay High and Frame Delay Low registers). The  $F_{delay}$  value is programmed in the FDELAYH and FDELAYL registers.

The frame rate is given by:

$$Frame\ Rate = \frac{Hclk}{FN_{Hclk}}$$

### 6.5 Partial Frame Integration

In some cases it is desirable to reduce the time during which the pixels in the array are allowed to integrate incident light without changing the frame rate.

This is known as *Partial Frame Integration* and can be achieved by resetting pixels in a given row ahead of the row being selected for readout as shown in Figure 27. The number of  $Hclk$  clocks required to process a partial frame is given by:

$$FP_{Hclk} = RN_{Hclk} * I_{time}$$

Where:

$RN_{Hclk}$

is the number of  $Hclk$  clock cycles required to process & shift out one row of pixels.

$I_{time}$

a programmable value between 0 & 32767 representing the number of rows ahead of the current row to be reset. The  $I_{time}$  value is programmed in the ITIMEH and ITIMEL registers.

Note:

Upon system reset the partial frame integration is automatically enabled. It can be disabled by setting the *PrtFrmEn* bit in the ITIMECONFIG register to a logic 0 or by programming 0.

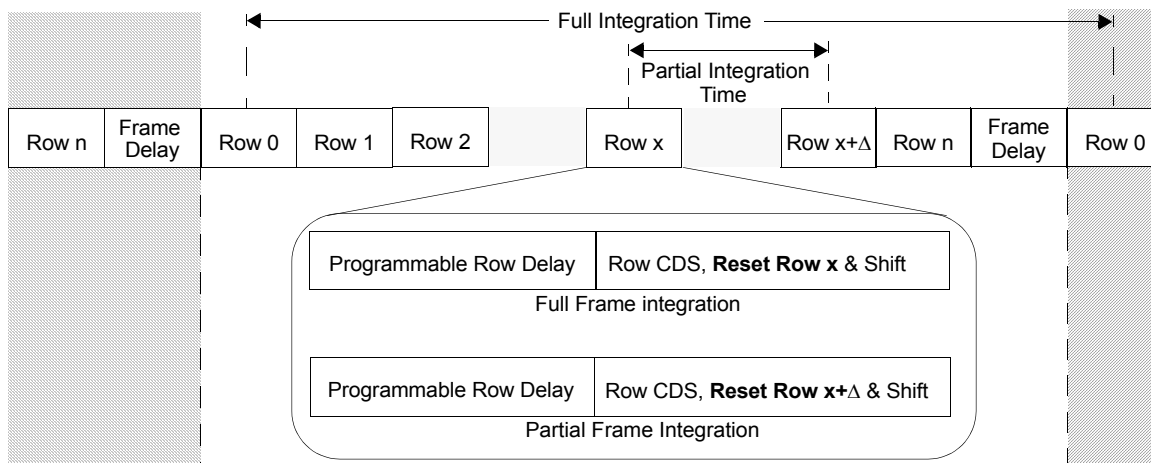


Figure 27. Partial and Full Frame Integration

## Functional Description (continued)

### 7.0 SNAPSHOT MODE

#### 7.1 Introduction

Two dedicated pins are provided on the KAC-9638, **snapshot**, and **extsync** allowing the sensor to be externally controlled to capture a single image. The **snapshot** input pin is used to trigger a snapshot, while the **extsync** output pin is used to synchronize a light source, strobe or mechanical shutter. Note that partial frame integration is not possible in snapshot mode.

#### 7.2 Taking a Snapshot

By default the sensor will operate in the **VIDEO** state (see figure 28). To take a snapshot, the snapshot mode must be enabled by setting the *SnapEnable* bit in the SNAPMODE register to a logic 1. This will cause the sensor to enter the **FREEZE** state at the end of the current frame. In the **FREEZE** state the sensor is idle. The sensor will leave the **FREEZE** state and return to **VIDEO** state when the snapshot mode is disabled (*SnapEnable* bit in the SNAPMODE register set to a logic 0).

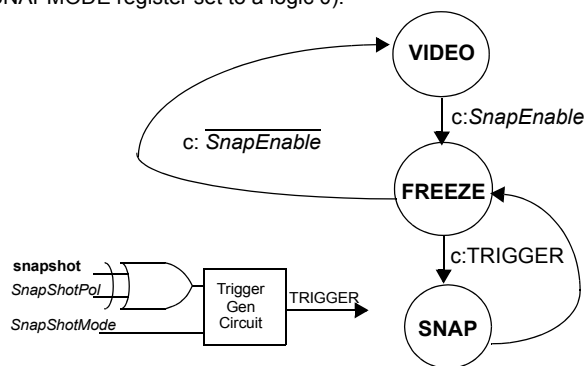


Figure 28. Snapshot Mode

Alternatively when an active snapshot signal is applied to the snapshot input pin an internal trigger signal, *TRIGGER*, is generated as shown in figure 28. The signal applied to the snapshot pin must be longer than 1 frame. The trigger generation circuit will create two types of *TRIGGER* as follows:

- **Pulse Trigger** (*SnapShotMode* bit of the SNAPMODE register is cleared). In this mode (the default) a single *TRIGGER* pulse will be generated.
- **Level Trigger** (*SnapShotMode* bit of the SNAPMODE register is set). In this mode the *TRIGGER* will remain high as long as the active level is held on the **snapshot** pin.

When a *TRIGGER* is generated the sensor will enter the **SNAP** state as shown in figure 28.

#### 7.3 The SNAP State in External Shutter Mode

To take a snapshot in external shutter mode, the *ShutterMode* bit of the SNAPMODE register must be set.

In this mode three consecutive operations will be carried out in the **SNAP** state as follows (see figure 29):

- **Array Reset**, during which the **extsync** pin is kept in-active and the array is reset one row at a time. The number of times the array is reset is programmable from 1-8 frames, (see the *SsFrames* bits in the SNAPMODE register).
- **Image Capture**, the **extsync** pin will activate. The width of the **extsync** signal can be programmed from 0 to 32767 lines by programming the snapshot integration time registers, *SNAPITH* and *SNAPITL*.
- **Array Read Out**, the third and final operation reads the image data out one row at a time.

#### 7.4 The SNAP State in Normal Mode (default)

To take a snapshot in normal mode, the *ShutterMode* bit of the SNAPMODE register must be cleared. In this case the following consecutive operations will be carried out in the **SNAP** state (see figure 29b and figure 29c):

- **Array Reset**, during which the **extsync** pin is kept in-active and the array is reset one row at a time. The number of times the array is reset is programmable from 1-8 frames, (see the *SsFrames* bits in the SNAPMODE register).
- **Image Capture**, the **extsync** pin will activate and remain active for the duration of the capture time. The length of the capture time can be programmed from 0 to 32767 lines by programming the snapshot integration time registers, *SNAPITH* and *SNAPITL*.
- **Array Read Out**, the image data is read out one row at a time. During this operation the **extsync** pin remains active.

#### 7.5 Return to the FREEZE State

When read out is complete the sensor will return to the **FREEZE** state.

#### 7.6 Return to the VIDEO state

If the snapshot mode is disabled before readout is complete (*SnapEnable* bit in the SNAPMODE register is set to a logic 0), then the sensor will return to the **VIDEO** state at the end of read-out.

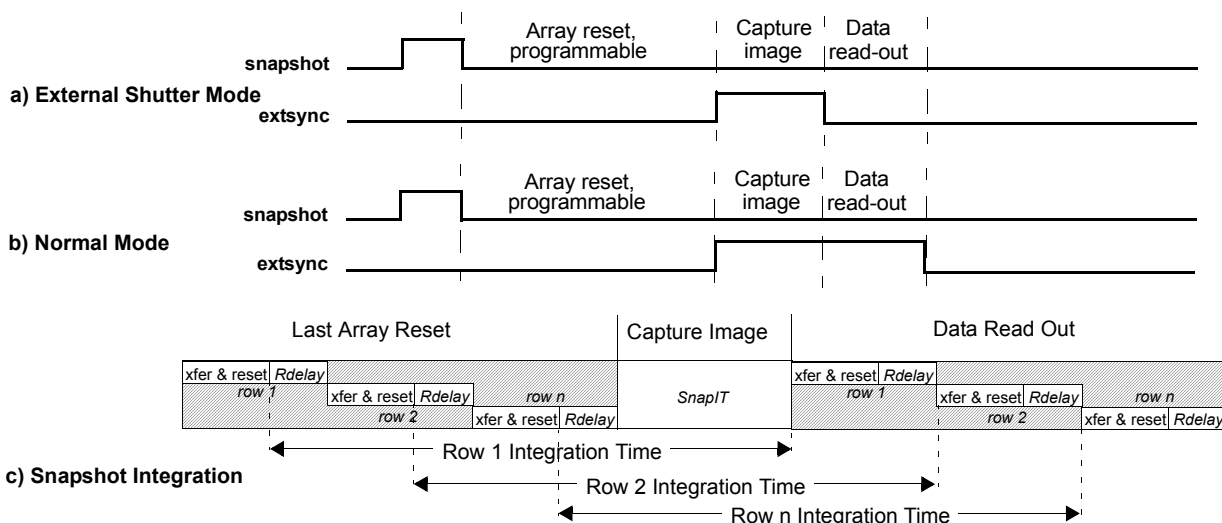


Figure 29. Snapshot Sequences

## Functional Description (continued)

### 8.0 BLACK LEVEL & OFFSET ADJUSTMENT

The KAC-9638 allows for both fine and coarse black level adjustment. Coarse adjustment is made using the `PIXELOFFSET` register and only needs to be done once at power up. Fine offset adjustment is done on a row basis and can be accomplished either automatically using the on chip black level compensation circuit or manually by disabling the on chip black level compensation circuit.

#### 8.1 Coarse Black Level and Offset Adjustment

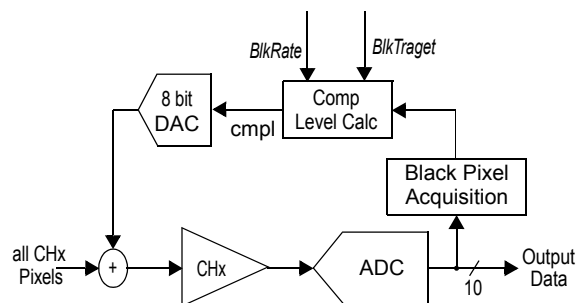
To ensure maximum performance of the CMOS image sensor, the natural offset of the pixel array needs to be minimized. Coarse adjustment is made using the `PIXELOFFSET` register and only needs to be done once at power up. This procedure is explained in detail in KAC-9648 Application Note 4.

#### 8.2 Manual Black Level and Offset Adjustment

The offset channel can provide up to 255 levels of black level and offset adjustment. To manually adjust the black level and offset the `BlkLevEn` bit in the `BLKLEVCONFIG` register should be set to a logic 1. Eight bit offset values can then be programmed to register `OFFSET`.

#### 8.3 Auto Black Level and Offset Adjustment

Automatic black level and offset adjustment mode is enabled by setting the `BlkLevEn` bit in the `BLKLEVCONFIG` register to a logic 0.



**Figure 30: Digital Black Level & Offset Adjustment Loop**

Figure 30 illustrates the automatic black level and offset compensation circuit contained within the sensor. For every row, the digitized values of the middle 8 black pixels (of the 24 columns of black pixels) are acquired and fed to the compensation level calculator circuit. This circuit is a digital first order exponential averaging filter. It calculates the compensation level (`cmpl`) that is required to ensure that for pixels that are optically black, the black level at the output of the ADC is equal to the desired black level. The desired black level (`ClkTarget`) can be programmed in the `BLKTARGET` register.

The black level control loop not only controls the black level of the pixels in the sensor array, but also controls the offset of the PGA and A/D in the system. The convergence rate of the cancellation loop can be set by programming the `BlkRate` parameter located in the `BLKLEVCONFIG` register. Small values of the `BlkRate` parameter ensure a fast convergence. High values of the `BlkRate` parameter reduce the noise in the calculated compensation level. The optimal setting of the `BlkRate` parameter is the result of a compromise between convergence speed after power up and image quality.

### 9.0 SYSTEM MANAGEMENT

#### 9.1 System Reset

Upon power up an on-chip power on reset block will ensure that the sensor is initialized to its reset state. After power up the sensor can be reset by asserting a logic 0 on the `resetb` pin or by writing to the `SenReset` bin in the `PWD&RST` register.

Furthermore, all state machines contained in the sensors integrated timing and control block can be reset by writing to the `RstzSoft` bit in the `OPCTRL` register.

#### 9.2 Power Up and Down

The KAC-9638 is equipped with an on-board power management system allowing the analog and digital circuitry to be switched off (power down) and on (power up) at any time.

The sensor can be put into power down mode by asserting a logic one on the `pwn` pin or by writing to the `PwDn` bit in the `PWD&RST` register.

To power up the sensor a logic zero can be asserted on the `pwn` pin or by writing to the `PwDn` bit in the `PWD&RST` register.

It will take a few milliseconds for all the circuits to power up. The power management register contains a bit indicating when the sensor is ready for use. During this time the sensor cannot be used for capturing images. A status bit in the power management register will indicate when the sensor is ready for use.

To ensure minimum power down currents, the internal bandgap circuit should be turned off before powering down the sensor.

To switch off the sensor's internal bandgap, the following sequence of codes should be written to the sensor via the I<sup>2</sup>C compatible interface before power down

| Address (Hex) | Data (Hex) |
|---------------|------------|
| INTREG2       | 01         |
| POWCTRL       | 82         |

Before the sensor can be powered up the its internal bandgap needs to be switched back on.

To switch the sensor's internal bandgap circuit on, the following sequence needs to be applied to the I<sup>2</sup>C compatible interface after power up to ensure correct operation.

| Address (Hex) | Data (Hex) |
|---------------|------------|
| POWCTRL       | 86         |
| OPCTRL        | 07         |
| INTREG2       | 00         |

## Functional Description (continued)

### 10.0 SERIAL BUS

The serial bus interface consists of the **sda** (serial data), **sclk** (serial clock) and **sadr** (device address select) pins. The KAC-9638 I2C interface can operate only as a slave.

The **sclk** pin is an input, it only controls the serial interface, all other clock functions within KAC-9638 use the master clock pin, **mclk**. **Mclk** must be active and at least 4 times faster than **sclk** for the serial interface to work properly.

#### 10.1 Start/Stop Conditions

The serial bus will recognize a logic 1 to logic 0 transition on the **sda** pin while the **sclk** pin is at logic 1 as the **start** condition. A logic 0 to logic 1 transition on the **sda** pin while the **sclk** pin is at logic 1 is interrupted as the **stop** condition as shown in Figure 31.

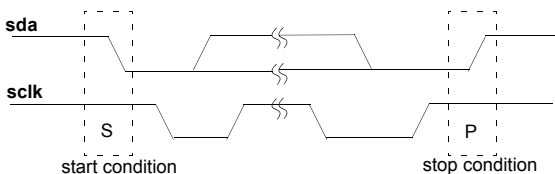


Figure 31. Start/Stop Conditions

#### 10.2 Device Address

The serial bus *Device Address* of the KAC-9638 is set to 1010101 when **sadr** is tied low and 0110011 when **sadr** is tied high. The value for **sadr** is set at power up.

The *Device Address* can be changed by writing to the *I2cDevAddr* parameter in the I2CMODE Register.

#### 10.3 Acknowledgment

The KAC-9638 will hold the value of the **sda** pin to a logic 0 during the logic 1 state of the *Acknowledge* clock pulse on **sclk** as shown in Figure 32.

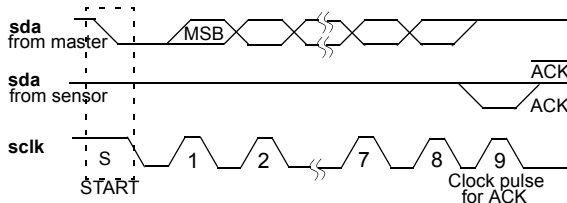


Figure 32. Acknowledge

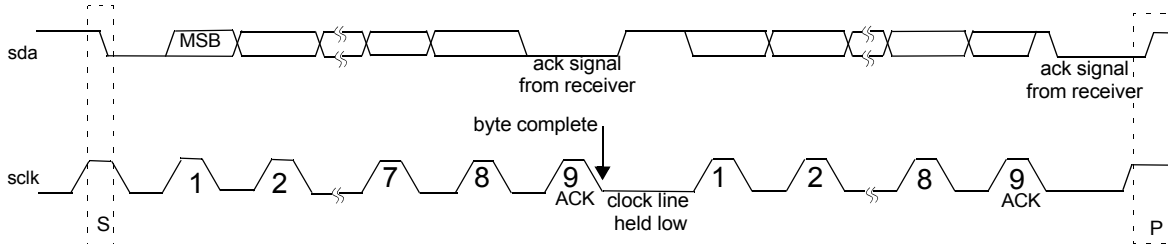
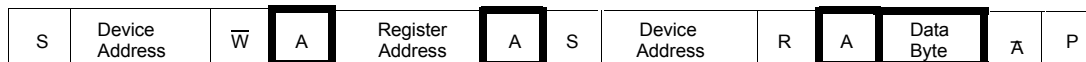


Figure 34. Serial Bus Byte Format



bold sensor action

Figure 35. Serial Bus Write Operation



bold sensor action

Figure 36. Serial Bus Read Operation

#### 10.4 Data Valid

The master must ensure that data is stable during the logic 1 state of the **sclk** pin. All transitions on the **sda** pin can only occur when the logic level on the **sclk** pin is "0" as shown in Figure 33

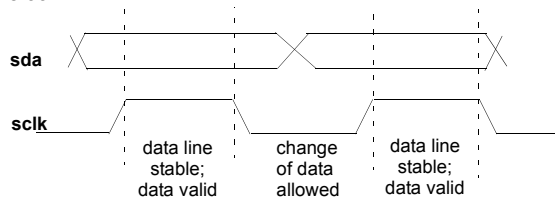


Figure 33. Data Validity

#### 10.5 Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an *Acknowledge*. The most significant bit of the byte is should always be transmitted first. See Figure 34.

#### 10.6 Write Operation

A write operation is initiated by the master with a *Start Condition* followed by the sensor's *Device Address* and *Write* bit. When the master receives an *Acknowledge* from the sensor it can transmit an 8-bit internal register address. The sensor will respond with a second *Acknowledge* signaling the master to transmit 8 write data bits. A third *Acknowledge* is issued by the sensor when the data has been successfully received. The write operation is completed when the master asserts a *Stop Condition* or a second *Start Condition*. See Figure 35.

#### 10.7 Read Operation

A read operation is initiated by the master with a *Start Condition* followed by the sensor's *Device Address* and *Write* bit. When the master receives an *Acknowledge* from the sensor it can transmit the internal *Register Address* byte. The sensor will respond with a second *Acknowledge*. The master must then issue a new *Start Condition* followed by the sensor's *Device Address* and *read* bit. The sensor will respond with an *Acknowledge* followed by the *Read Data* byte.

The read operation is completed when the master asserts a *Not Acknowledge* followed by *Stop Condition* or a second *Start Condition*. See Figure 36.

#### 10.8 Advanced Write Mode

Several addresses can be written to without the need to re-start by setting the *AdvWr* bit in the I2CMODE register to a logic 1.

## Functional Description (continued)

### 11.0 DIGITAL VIDEO PORT

The captured image is placed onto a flexible 10-bit digital port as shown in Figure 10. The digital video port consists of a programmable 10-bit digital Data Out Bus (**d[9:0]**) and three programmable synchronisation signals (**hsync**, **vsync**, **pclk**).

By default the synchronisation signals are configured to operate in “slave” mode. They can be programmed to operate in “master” mode.

The following sections are a detailed description of the timing and programming modes of digital video port.

The 10-bit digital video out bus can be tri-stated by asserting a logic 0 on the **oe** pin or by writing a logic 1 to the *TriState* bit in the DVBUSCONFIG3 register.

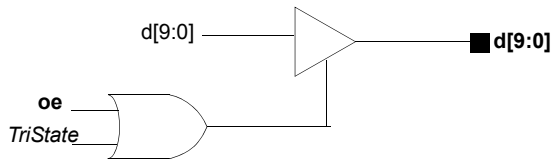


Figure 37. Digital Pixel Data Out Bus Circuit Diagram

#### 11.1 Digital Video Data Out Bus (d[9:0])

A programmable barrel shifter is provided to map the output of the internal pixel data framer to the pins of the digital video bus as illustrated in Figure 38.

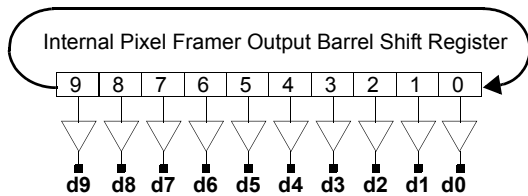


Figure 38. Digital Video Bus Switching Modes

The *Bshift* parameter in the DVBUSCONFIG2 register can be used to program the number of bits that the digital pixel data is shifted by.

This feature allows a programmable digital gain to be implemented when connecting the sensor to 8 or 10 bit digital video processing systems as illustrated in Figure 39.

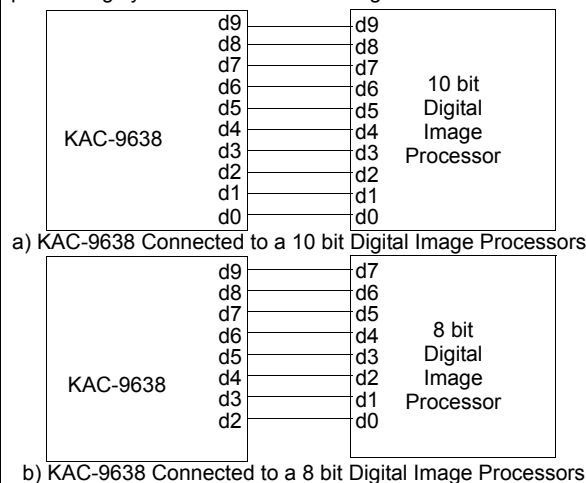


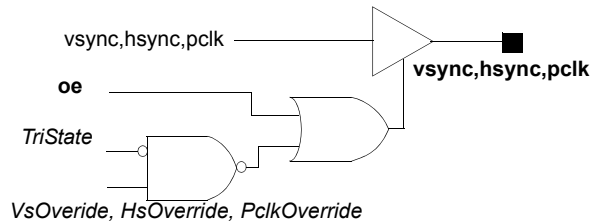
Figure 39. Example of connection to 10/8 bit systems

### 11.2 Synchronisation Signals in Master Mode

In master mode the integrated timing and control block controls the flow of data onto the 10-bit digital port, three synchronisation outputs are provided:

- pclk** is the pixel clock output pin.
- hsync** is the horizontal synchronisation output signal.
- vsync** is the vertical synchronisation output signal.

The **vsync**, **hsync** and **pclk** signals can be tri-stated by asserting a logic 0 on the **oe** pin or by writing a logic 0 to the *TriState* bit in the DVBUSCONFIG3 register. (see figure 40) The tristating of **Vsync**, **Hsync**, and **Pclk** can be overridden by setting the appropriate bit in the DVBUSCONFIG3 register.



*VsOverride*, *HsOverride*, *PclkOverride*

Figure 40. hsync, vsync and pclk output circuit diagram

#### 11.3 Pixel Clock Output Pin (pclk) (Master Mode)

The pixel clock output pin, **pclk**, is provided to act as a synchronisation reference for the pixel data appearing at the digital video out bus pins **d[9:0]**. This pin can be programmed to operate in two modes:

- In free running mode, (the *PixClkMode* bit of DVBUSCONFIG1 register is set to a logic 0), the pixel clock output pin, **pclk**, is always running with a fixed period. Pixel data appearing on the digital video bus **d[9:0]** are synchronized to a specified active edge of the clock as shown in Figure 41.

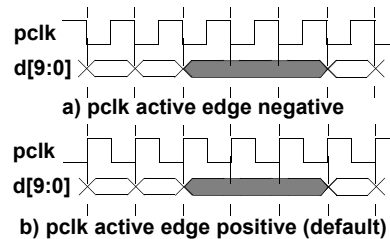


Figure 41. pclk in Free Running Mode

- In data ready mode, (the *PixClkMode* bit of DVBUSCONFIG1 register is set to a logic 1), the pixel clock output pin **pclk** will produce a pulse with a specified level every time valid pixel data appears on the digital video bus **d[9:0]** as shown in Figure 42.

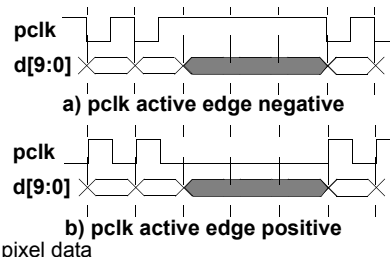


Figure 42. pclk in Data Ready Mode

## Functional Description (continued)

By default the pixel clock is a free running active high (pixel data changes on the positive edge of the clock) with a period equal to the internal *hclk*. See section 6.3 for more *pclk* programming modes.

### 11.4 Horizontal Synchronisation Output Pin (*hsync*)

The horizontal synchronisation output pin, *hsync*, is used as an indicator for row data. The *hsync* output pin can be programmed to operate in two modes as follows:

- **Level mode** should be used when the pixel clock, *pclk*, is programmed to operate in *free running mode*. In level mode the *hsync* output pin will go to the specified level (high or low) at the start of each row and remain at that level until the last pixel of that row is read out on *d[9:0]* as shown in Figure 43. The *hsync* level is always synchronized to the active edge of *pclk*. The *hsync* pin is put into level mode by setting the *HsyncMode* bit of the *DVBUSCONFIG1* register to a logic 0. The active level of the *hsync* pulse is programmed using the *HsyncPol* bit of the *DVBUSCONFIG1* register.

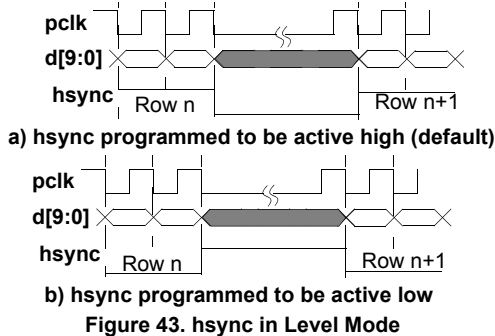


Figure 43. *hsync* in Level Mode

- **Pulse mode** should be used when the pixel clock, *pclk*, is programmed to operate in *data ready mode*. In pulse mode the *hsync* output pin will produce a pulse at the end of each row. The width of the pulse will be a minimum of four *pclk* cycles and its polarity can be programmed as shown in Figure 44. The *hsync* level is always synchronized to the active edge of *pclk*. The *hsync* pin is put into pulse mode by setting the *HsyncMode* bit of the *DVBUSCONFIG1* register to a logic 1. The active level of the *hsync* pulse is programmed using the *HsyncPol* bit of the *DVBUSCONFIG1* register.

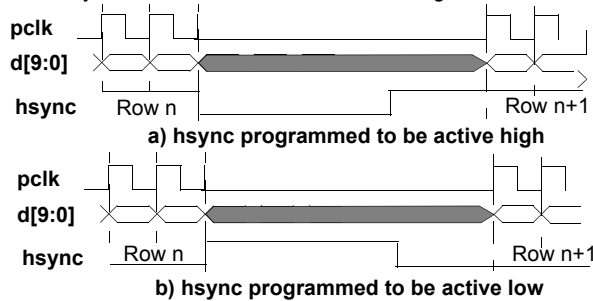


Figure 44. *hsync* in Pulse Mode

By default the first pixel data at the beginning of each row is placed on the digital video bus as soon as *hsync* is activated. Furthermore, *hsync* is de-activated upon the placement of the last pixel of the current row on the digital video bus. It is possible to shift the start and end edges of the *hsync* signal by programming the *HsyncStart* parameter of the *DVBUSCONFIG0* register and the *HsyncEnd* parameter of the *HSYNCAJUST* register.

### 11.5 Vertical Synchronisation Pin (*vsync*)

The vertical synchronisation output pin, *vsync*, is used as an indicator for pixel data within a frame. The *vsync* output pin can be programmed to operate in two modes as follows:

- **Level mode** should be used when the pixel clock, *pclk*, is programmed to operate in *free running mode*. In level mode the *vsync* output pin will go to the specified level (high or low) at the start of each frame and remain at that level until the last pixel of the last row in the frame is placed on *d[9:0]* as shown in Figure 45. The *vsync* level is always synchronized to the active edge of *pclk*. The *vsync* pin is put into level mode by setting the *VsyncMode* bit of the *DVBUSCONFIG1* register to a logic 0. The active level of the *vsync* is programmed using the *VsyncPol* bit of the *DVBUSCONFIG1* register.

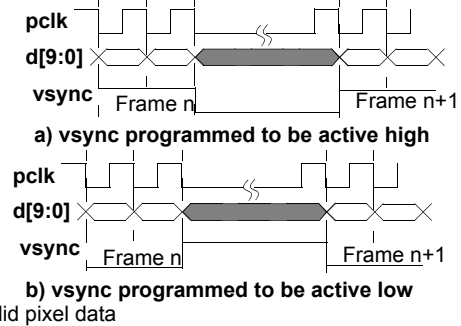


Figure 45. *vsync* in Level Mode

- **Pulse mode** should be used when the pixel clock, *pclk*, is programmed to operate in *data ready mode*. In pulse mode the *vsync* output pin will produce a pulse at the end of each frame. The width of the pulse will be a minimum of four *hclk* cycles and its polarity can be programmed as shown in Figure 46. The *vsync* level is always synchronized to the active edge of *pclk*. The *vsync* pin is put into pulse mode by setting the *VsyncMode* bit of the *DVBUSCONFIG1* register to a logic 1. The active level of the *vsync* pulse is programmed using the *VsyncPol* bit of the *DVBUSCONFIG1* register.

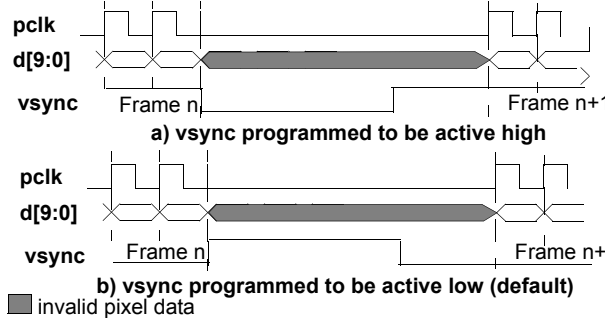


Figure 46. *vsync* in Pulse Mode

By default the first pixel data at the beginning of each frame is placed on the digital video bus as soon as *vsync* is activated. Furthermore, *vsync* is de-activated upon the placement of the last pixel of the current frame on the digital video bus. It is possible to shift the start and end edges of the *vsync* signal by programming the *VsyncStart* parameter of the *DVBUSCONFIG0* register and the *VsyncEnd* parameter of the *VSYNCAJUST* register.

**Functional Description** (continued)

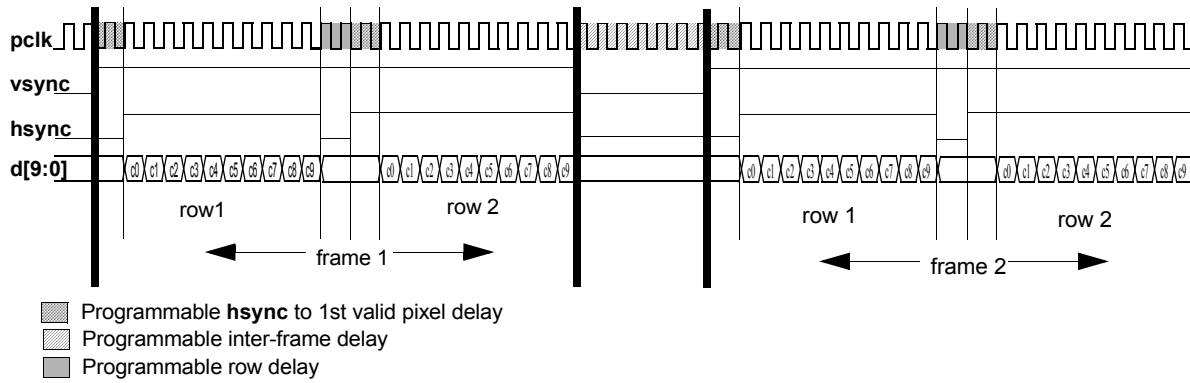


Figure 47. Example of Digital Video Port Timing

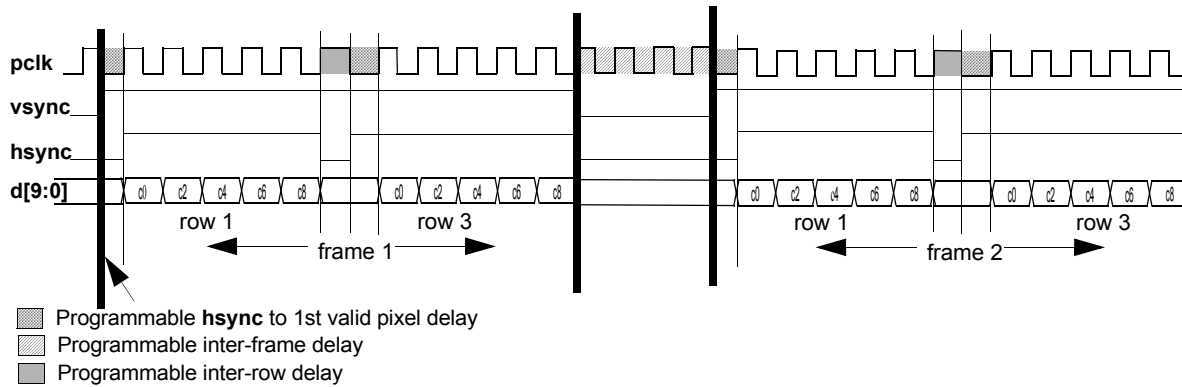


Figure 48. Example of Digital Video Port Timing in 2:1 Sub-sampling Mode

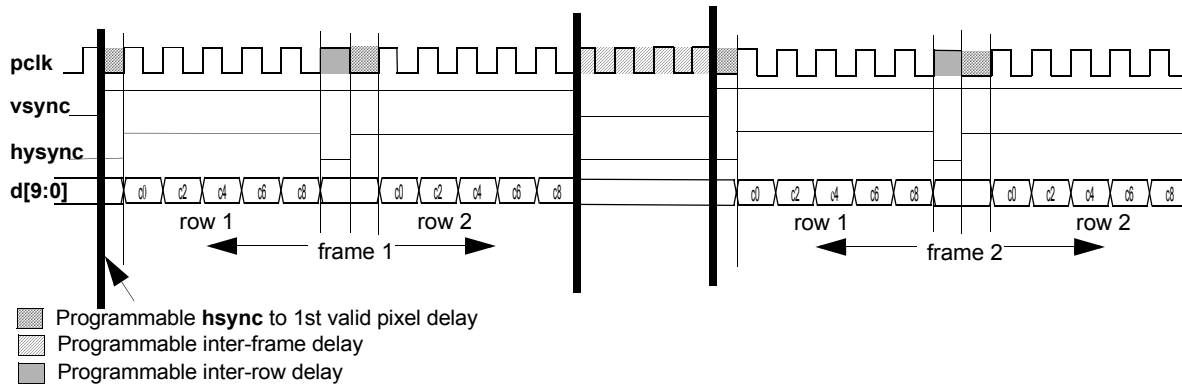


Figure 49. Example of Digital Video Port Timing in 4:2 Sub-sampling Mode

## Functional Description (continued)

### 11.6 Synchronisation Signals in Slave Mode

By default the sensor's digital video port's synchronisation signals are configured to operate in slave mode. In slave mode the integrated timing and control block will only start frame and row processing upon the receipt of triggers from an external source. Partial Frame integration is disabled in this mode. Only two synchronization signals are used in slave mode as follows:

- hsync** is the row trigger input signal.
- vsync** is the frame trigger input signal.

Figure 50 shows the KAC-9638's digital video port in slave mode connected to a digital video processor master DVP.

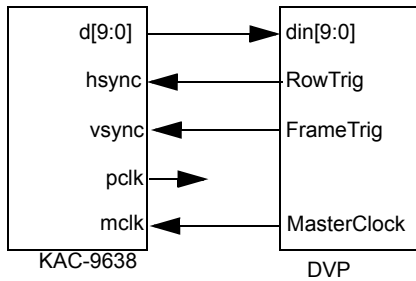


Figure 50. KAC-9638 in slave mode

### 11.7 Row Trigger Input Pin (hsync)

The row trigger input pin, **hsync**, is used to trigger the processing of a given row. It must be activated for at least two **mclk** cycles. The first pixel data will appear at **d[9:0]**  $X_{pclk}$  periods after the assertion of the row trigger, where  $X_{pclk}$  is given by:

$$X_{pclk} = 147 + 100 \cdot HAvrg - 8 \cdot BlkPixelEn$$

Where:

*HAvg* is the HAvrg bit setting in the VSCAN register.  
*BlkPixelEn*

is the BlkPixelEn bit setting in the DVBUSCONFIG2 register

The polarity of the active level of the row trigger can be programmed using the HsynPol bit of the DVBUSCONFIG1 register. By default it is active high.

### 11.8 Frame Trigger Input Pin (vsync)

The frame trigger input pin, **vsync**, is used to reset the row address counter and prepare the array for row processing. It must have a duration of at least two **mclk** cycles and must be activated at least 20 **pclk** cycles after the activation of the last **hsync** of the previous frame as illustrated in Figure 52.

The polarity of the active level of the row trigger is programmable. By default it is active high.

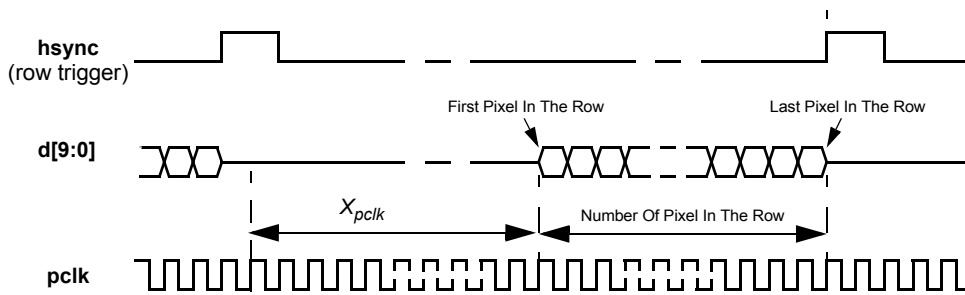


Figure 51. hsync slave mode timing diagram for centred display window of 642 pixels

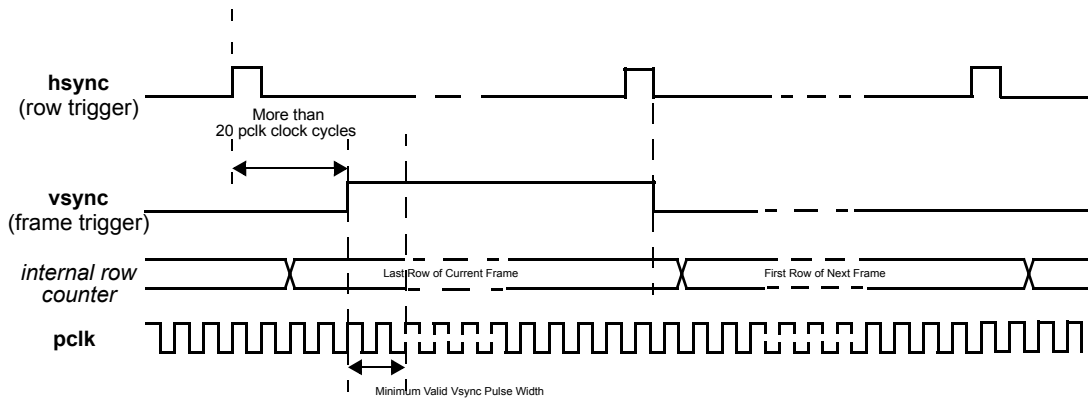


Figure 52. vsync slave mode timing diagram.



## MEMORY MAP

| ADDR       | Register     | Reset Value | Description   |
|------------|--------------|-------------|---|
| 00h        | DEVID        | 48h         | Device ID Register.   |
| 01h        | REV          | 09h         | Revision Register   |
| 02h - 04h  |              |             | Reserved  |
| 05h        | VCLKGEN      | 00h         | Clock Generation Register   |
| 06h        | PWD&RST      | 00h         | Power Down & Reset Register   |
| 07h        | I2CMODE      | AAh         | I <sup>2</sup> C compatible Serial Interface Configuration Register |
| 08h        |              |             | Reserved  |
| 09h        | OPCTRL       | 06h         | Operation Control Register  |
| 0Ah - 0Fh  |              | 00h         | Reserved  |
| 10h        | VIDCONFIG    | 01h         | Video Color Configuration Register                                  |
| 11h        | VSCAN        | 04h         | Vertical Scan Configuration Register                                |
| 12         |              |             | Reserved  |
| 13h        | HSCAN        | 04h         | Horizontal Scan Configuration Register                              |
| 14h        |              |             | Reserved  |
| 15h        | ITIMECONFIG  | 08h         | Integration Time Configuration Register                             |
| 16h-18h    |              |             | Reserved  |
| 19h        | WROWS        | 00h         | Active Window Row Start Register                                    |
| 1Ah        | WROWE        | 80h         | Active Window Row End Register                                      |
| 1Bh        | WROWLSB      | 23h         | Active Window Row LSB Register                                      |
| 1Ch        | WCOLS        | 00h         | Active Window Column End Register                                   |
| 1Dh        | WCOLE        | A0h         | Active Window Column Start Register                                 |
| 1Eh        | WCOLLSB      | 23h         | Active Window Column LSB Register                                   |
| 20h        | FDELAYH      | 00h         | Frame Delay High Register   |
| 21h        | FDELAYL      | 08h         | Frame Delay Low Register  |
| 22h        | RDELAYH      | 00h         | Row Delay High Register   |
| 23h        | RDELAYL      | 08h         | Row Delay Low Register  |
| 24h        | ITIMEH       | 00h         | Integration Time High Register                                      |
| 25h        | ITIMEL       | 00h         | Integration Time Low Register                                       |
| 26h - 2Fh  |              |             | Reserved  |
| 30h        | SNAPMODE     | 07h         | Snapshot Mode Configuration Register                                |
| 31h        | SNAPITH      | 1Fh         | Snapshot High Integration Time Register                             |
| 32h        | SNAPITL      | 7Fh         | Snapshot Low Integration Time Register                              |
| 33h - 3Fh  |              |             | Reserved  |
| 40h        | BLKLEVCONFIG | 07h         | Black Level Compensation Register                                   |
| 41h        | BLKTARGET    | 10h         | Black Level Target Register   |
| 42h        | PGA          | 00h         | Programmable Gain Amplifier   |
| 43h - 45fh |              |             | Reserved For The KAC-9648. Must be set to 00 Hex                    |
| 46h        | OFFSET       | 00h         | Gain Offset Register  |
| 47h - 4Ah  |              |             | Reserved For the KAC-9648. Must be set to 00 Hex.                   |
| 4Bh- 4Fh   |              |             | Reserved  |

**MEMORY MAP** (continued)

| ADDR      | Register     | Reset Value | Description                                |
|-----------|--------------|-------------|--|
| 50h       | VSYNCADUST   | 08h         | Vsync Adjust Register                      |
| 51h       | HSYNCADUST   | 08h         | Hsync Adjust Register                      |
| 52h       | DVBUSCONFIG0 | 00h         | Digital Video Bus Configuration Register 0 |
| 53h       | DVBUSCONFIG1 | 0Ch         | Digital Video Bus Configuration Register 1 |
| 54h       | DVBUSCONFIG2 | F0h         | Digital Video Bus Configuration Register 2 |
| 55h       | DVBUSCONFIG3 | 00h         | Digital Video Bus Configuration Register 3 |
| 56h - 7Fh |              |             | Reserved                                   |
| 80h       | INTREG1      | 00h         | Sensor Initialization Register 1           |
| 81h - 82h |              |             | Reserved                                   |
| 83h       | PIXELOFFSET  | 1Eh         | Sensor's Pixel Offset Register             |
| 84h       |              |             | Reserved                                   |
| 85h       | POWCTRL      | 81h         | Sensor's Power Down Control Register       |
| 86h - 87h |              |             | Reserved                                   |
| 88h       | INTREG2      | 00h         | Sensor Initialization Register 2           |

## Register Set

The following section describes all available registers in the KAC-9638 register bank and their function.

**Register Name** Device ID  
**Address** 00 Hex  
**Mnemonic** DEVID  
**Type** Read Only  
**Reset Value** 48 Hex

| Bit | Bit Symbol | Description             |
|-----|------------|-------------------------|
| 7:0 | DevId      | The sensor's device ID. |

**Register Name** Silicon Revision  
**Address** 01 Hex  
**Mnemonic** REV  
**Type** Read Only  
**Reset Value** 09 Hex

| Bit | Bit Symbol | Description                    |
|-----|------------|--------------------------------|
| 7:0 | SiRev      | The sensor's silicon revision. |

**Register Name** Clock Generation Register  
**Address** 05 Hex  
**Mnemonic** VCLKGEN  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol  | Description   |   |             |   |    |
|-----|-------------|---|---|-------------|---|----|
| 7   |             | Reserved.   |   |             |   |    |
| 2   |             | Reserved  |   |             |   |    |
| 1   | HclkGen     | Use to divide the frequency of the sensors master clock input, <b>mclk</b> , and generate the sensor's internal clock, <b>hclk</b> .<br><br><table border="1" style="margin-left: 20px;"> <tr> <td>0</td> <td>÷1(default)</td> </tr> <tr> <td>1</td> <td>÷2</td> </tr> </table> | 0 | ÷1(default) | 1 | ÷2 |
| 0   | ÷1(default) |   |   |             |   |    |
| 1   | ÷2          |   |   |             |   |    |
| 0   |             | Reserved.   |   |             |   |    |

**Register Name** Power Down/Reset Register  
**Address** 06 Hex  
**Mnemonic** PWD&RST  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:2 |            | Reserved.  |
| 1   | SenReset   | Set this self clearing bit to a logic 1 to reset the sensor.   |
| 0   | PwDn       | Set to a logic 1 to power down the chip. All internal clocks will be turned off in this mode.<br><br>Set to a logic 0, (the default) to put the chip in power up mode.<br><br>Refer to section 9.2 for information on the low power down sequence. |

**Register Name** I<sup>2</sup>C Mode Register  
**Address** 07 Hex  
**Mnemonic** I2CMODE  
**Type** Read/Write  
**Reset Value** AA Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:1 | I2cDevAddr | Use to program the I <sup>2</sup> C compatible device address. By default, the value is 55 hex.  |
| 0   | AdvWr      | Set to a logic 1 to activate the I <sup>2</sup> C compatible serial interface's advance write option. In advance write mode, several addresses can be written to without the need to restart.<br><br>Set to a logic 0, the default, to operate the I <sup>2</sup> C compatible interface in standard write mode. |

**Register Name** Operation Control Register  
**Address** 09 Hex  
**Mnemonic** OPCTRL  
**Type** Read/Write  
**Reset Value** 06 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:3 |            | Reserved.  |
| 3   | LowLight   | Set to a logic 1 to configure the analog gain amplifiers to high gain mode for low light conditions.<br><br>Set to a logic 0 (the default) to configure the analog gain amplifiers for normal light conditions.                          |
| 2   | MasterMode | Set to a logic 1 to configure the digital video port's synchronisation's signal to operate in master mode.<br><br>Set to a logic 0 (the default) to configure the digital video port's synchronisation signals to operate in slave mode. |
| 1   |            | This bit is reserved for factory testing and must be set to a logic 1 at all times.  |
| 0   | RstzSoft   | Set this self clearing register to a logic 1 to reset all state machines contained in the integrated smart timing and control circuitry.   |

### Register Set (continued)

**Register Name** Video Configuration Register  
**Address** 10 Hex  
**Mnemonic** VIDCONFIG  
**Type** Read/Write  
**Reset Value** 01 Hex.

| Bit | Bit Symbol | Description   |
|-----|------------|---|
| 7:1 |            | Reserved.   |
| 0   | Color      | Set to a logic 1, (the default), to configure the sensor's smart timing and control circuit to operate in color mode. This bit always be set for color sensor.<br><br>Set to a logic 0 to configure the sensor's smart timing and control circuit to operate in mono-chrome mode. |

**Register Name** Vertical Scan Register  
**Address** 11 Hex  
**Mnemonic** VSCAN  
**Type** Read/Write (Double Buffered)  
**Reset Value** 04 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:3 |            | Reserved.  |
| 2   | VscanDir   | Set to a logic 1, (the default), to set the sensor's vertical scan direction to operate from top to bottom.<br><br>Set to a logic 0, to set the sensor's vertical scan direction to operate from bottom to top.  |
| 1   | VSub       | Set to a logic 1 to enable vertical sub sampling.<br><br>Set to a logic 0, (the default), to disable vertical sub sampling.  |
| 0   | VAvg       | Set to a logic 1 to enable vertical averaging.<br><br>Set to a logic 0, (the default) to disable vertical averaging.<br><br>Note setting this bit to a logic 1 overrides the logic level of the <i>Vsub</i> bit, automatically enabling vertical sub-sampling. |

**Register Name** Horizontal Scan Register  
**Address** 13 Hex  
**Mnemonic** HSCAN  
**Type** Read/Write (Double Buffered)  
**Reset Value** 04 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:3 |            | Reserved.  |
| 2   | HscanDir   | Set to a logic 1, (the default) to set the sensor's horizontal scan direction to operate from left to right.<br><br>Set to a logic 0, to set the sensor's horizontal scan direction to operate from right to left.   |
| 1   | HSub       | Set to a logic 1 to enable horizontal sub sampling.<br><br>Set to a logic 0, (the default), to disable horizontal sub sampling.  |
| 0   | HAvg       | Set to a logic 1 to enable horizontal averaging.<br><br>Set to a logic 0, (the default) to disable horizontal averaging.<br><br>Note setting this bit to a logic 1 overrides the logic level of the <i>Hsub</i> bit, automatically enabling horizontal sub-sampling. |

**Register Name** Integration Time Configuration Register  
**Address** 15 Hex  
**Mnemonic** ITIMECONFIG  
**Type** Read/Write (Double Buffered)  
**Reset Value** 08 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:4 |            | Reserved.  |
| 3   | PrtFrmEn   | Set to a logic 1, (the default), to turn on the Partial Frame Integration.<br><br>Set to a logic 0, to turn off the partial Partial Frame Integration. |
| 2:0 |            | Reserved, should always be set to a logic 0.   |

### Register Set (continued)

**Register Name** Active Window Row Start Register  
**Address** 19 Hex  
**Mnemonic** WROWS  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol       | Description   |
|-----|------------------|---|
| 7:0 | WStartRow [10:3] | Use to program the display window's start row address' MSBs. The LSBs can be programmed using the WROWLSB register. |

**Register Name** Active Window Row End Register  
**Address** 1A Hex  
**Mnemonic** WROWE  
**Type** Read/Write (Double Buffered)  
**Reset Value** 80 Hex.

| Bit | Bit Symbol     | Description  |
|-----|----------------|--|
| 7:0 | WEndRow [10:3] | Use to program the scan window's end row address' MSBs. The LSBs can be programmed using the WROWLSB register. |

**Register Name** Active Window Row LSB Register  
**Address** 1B Hex  
**Mnemonic** WROWLSB  
**Type** Read/Write (Double Buffered)  
**Reset Value** 23 Hex.

| Bit | Bit Symbol     | Description  |
|-----|----------------|--|
| 7:6 |                | Reserved   |
| 5   | WStartRow[2]   | Use to program the display window's start row address LSBs. The MSBs can be programmed using the WROWS register.                                 |
| 4:3 | WStartRow[1:0] | The two LSB's of the window start address are fixed to 0h. Although these bits can be written too they will have no effect on the window size.   |
| 2   | WEndRow[2]     | Use to program the scan window's end row address's LSBs. The MSBs can be programmed using the WROWE register                                     |
| 1:0 | WEndRow[1:0]   | The two LSB's fo the window row end address are fixed to 3h. Although these bits can be written too they will have no effect on the window size. |

**Note:** The row and column start and end registers should be written to at power up to guarantee that the expected window size is set.

**Register Name** Active Window Column Start Register  
**Address** 1C Hex  
**Mnemonic** WCOLS  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol       | Description  |
|-----|------------------|--|
| 7:0 | WStartCol [10:3] | Use to program the display window's start column address' MSBs. The LSBs can be programmed using the WCOLLSB register. |

**Register Name** Active Window Column End Register  
**Address** 1D Hex  
**Mnemonic** WCOLE  
**Type** Read/Write (Double Buffered)  
**Reset Value** A0 Hex.

| Bit | Bit Symbol     | Description   |
|-----|----------------|---|
| 7:0 | WEndCol [10:3] | Use to program the scan window's end column address' MSBs. The LSBs can be programmed using the WCOLLSB register. |

**Register Name** Active Window Column LSB Register  
**Address** 1E Hex  
**Mnemonic** WCOLLSB  
**Type** Read/Write (Double Buffered)  
**Reset Value** 23 Hex.

| Bit | Bit Symbol     | Description  |
|-----|----------------|--|
| 7:6 |                | Reserved   |
| 5   | WStartCol[2]   | Use to program the display window's start column address' LSBs. The MSBs can be programmed using the WCOLS register. |
| 4:3 | WStartCol[1:0] | The two LSBs of the window column start address WStartCol[1:0] are internally hard wired to 0 Hex.                   |
| 2   | WEndCol[2]     | Use to program the scan window's end column address' LSBs. The MSBs can be programmed using the WCOLE register.      |
| 1:0 | WEndCol[1:0]   | The two LSBs of the window column end are internally hard-wired to 3h.   |

**Register Set** (continued)

**Register Name** Frame Delay High Register  
**Address** 20 Hex  
**Mnemonic** FDELAYH  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol   | Description  |
|-----|--------------|--|
| 7:0 | Fdelay[14:7] | Use to program the MSBs of the frame delay. Note the max allowed frame delay is 32767. |

**Register Name** Frame Delay Low Register  
**Address** 21 Hex  
**Mnemonic** FDELAYL  
**Type** Read/Write (Double Buffered)  
**Reset Value** 08 Hex.

| Bit | Bit Symbol  | Description   |
|-----|-------------|---|
| 7   |             | Reserved.   |
| 6:0 | Fdelay[6:0] | Use to program the LSBs of the frame delay. Note the max allowed frame delay is 32767 |

**Register Name** Row Delay High Register  
**Address** 22 Hex  
**Mnemonic** RDELAYH  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol   | Description                               |
|-----|--------------|---|
| 7:0 | Rdelay[12:5] | Use to program the MSBs of the row delay. |

**Register Name** Row Delay Low Register  
**Address** 23 Hex  
**Mnemonic** RDELAYL  
**Type** Read/Write (Double Buffered)  
**Reset Value** 08 Hex.

| Bit | Bit Symbol  | Description                               |
|-----|-------------|---|
| 7:5 |             | Reserved.                                 |
| 4:0 | Rdelay[4:0] | Use to program the LSBs of the row delay. |

**Register Name** Integration Time High Register  
**Address** 24 Hex  
**Mnemonic** ITIMEH  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol  | Description  |
|-----|-------------|--|
| 7:4 |             | Reserved   |
| 3:0 | itime[10:7] | Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset. The maximum ITIME value is 1031. |

**Register Name** Integration Time Low Register  
**Address** 25 Hex  
**Mnemonic** ITIMEL  
**Type** Read/Write (Double Buffered)  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description   |
|-----|------------|---|
| 7   |            | Reserved.   |
| 6:0 | itime[6:0] | Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be resetThe maximum ITIME value is 1031.. |

### Register Set (continued)

**Register Name** Snapshot Mode Configuration Register  
**Address** 30 Hex  
**Mnemonic** SNAPMODE  
**Type** Read/Write (Double Buffered)  
**Reset Value** 07 Hex.

| Bit | Bit Symbol    | Description  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
|-----|---------------|--|-----|------------|-----|------------|-----|--------------|-----|-------------|-----|-------------|-----|------------|-----|--------------|-----|--------------|
| 7:6 |               | Reserved.  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 5   | SnapEnable    | Set to a logic 1 to configure the sensor to operate in snapshot mode. Set to a logic zero (the default) to operate the sensor in video mode.   |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 4   | Snapshot-Mode | Set to a logic 1 (the default) to operate the <b>snapshot</b> signal in pulse mode. In pulse mode the sensor will only carry out one snapshot sequence per pulse applied to the <b>snapshot</b> pin.<br><br>Set to a logic 0 to operate the <b>snapshot</b> pin to level mode. In level mode the sensor will continually run snapshot sequences as long as the <b>snapshot</b> pin is held to the active.  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 3   | ShutterMode   | Set to a logic 1 indicate that an external shutter will be used during snapshot mode.<br><br>Set to a logic 0, (the default) to indicate that snapshot mode will be carried out without the aid of an external shutter.  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 2:0 | SsFrames      | Program to set the number of frames required before readout during a snapshot with no external shutter, (see Figure 29). By default these three bits are set to 111 resulting in eight frames before readout:<br><br><table border="1"> <tr><td>000</td><td>one frames</td></tr> <tr><td>001</td><td>two frames</td></tr> <tr><td>010</td><td>three frames</td></tr> <tr><td>011</td><td>four frames</td></tr> <tr><td>100</td><td>five frames</td></tr> <tr><td>101</td><td>six frames</td></tr> <tr><td>110</td><td>seven frames</td></tr> <tr><td>111</td><td>eight frames</td></tr> </table> | 000 | one frames | 001 | two frames | 010 | three frames | 011 | four frames | 100 | five frames | 101 | six frames | 110 | seven frames | 111 | eight frames |
| 000 | one frames    |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 001 | two frames    |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 010 | three frames  |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 011 | four frames   |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 100 | five frames   |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 101 | six frames    |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 110 | seven frames  |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |
| 111 | eight frames  |  |     |            |     |            |     |              |     |             |     |             |     |            |     |              |     |              |

**Register Name** Snapshot Integration Time MSB Register  
**Address** 31 Hex  
**Mnemonic** SNAPITH  
**Type** Read/Write (Double Buffered)  
**Reset Value** 0F Hex.

| Bit | Bit Symbol   | Description  |
|-----|--------------|--|
| 7:0 | SnapIT[14:7] | Use to program the MSBs of the image capture time in snapshot mode, (see figure 29).<br><br>Note: when <i>SnapIT[14:0]</i> is set to 0000Hex, although no <b>extsync</b> pulse will result, image data will be output. |

**Register Name** Snapshot Integration Time LSB Register  
**Address** 32 Hex  
**Mnemonic** SNAPITL  
**Type** Read/Write (Double Buffered)  
**Reset Value** 7F Hex.

| Bit | Bit Symbol  | Description  |
|-----|-------------|--|
| 7   |             | Reserved.  |
| 6:0 | SnapIT[6:0] | Use to program the LSBs of the image capture time in snapshot mode, (see figure 29).<br><br>Note if <i>SnapIT[14:0]</i> is set to 0000Hex, no <b>extsync</b> pulse will result, image data will be output. |

**Register Name** Black Level Configuration Register  
**Address** 40 Hex  
**Mnemonic** BLKLEVCONFIG  
**Type** Read/Write  
**Reset Value** 07 Hex.

| Bit | Bit Symbol | Description   |
|-----|------------|---|
| 7   |            | Reserved.   |
| 3   | BlkLevEn   | Set to a logic 1 to disable the internal black level compensation circuit. Set to a logic 0, (the default) to enable the internal black level compensation circuit. |
| 2:0 | BlkRate    | Use to adjust the rate at which the auto black level circuit converges to the programmed target, <i>BlkTarget</i> . See section 8.3 for more information.           |

**Register Name** Reference Black Level Register  
**Address** 41 Hex  
**Mnemonic** BLKTARGET  
**Type** Read/Write  
**Reset Value** 10 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:0 | BlkRef     | Use to program the target black level. See section 8.3 for more information. |

### Register Set (continued)

**Register Name** PGA Register  
**Address** 42 Hex  
**Mnemonic** PGA  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7   |            | Reserved   |
| 6:0 | PGA        | Use to program the analog gain. Max gain is 16dB of gain programmable in 128 steps of 0.125dB. |

**Register Name** Offset Register  
**Address** 46 Hex  
**Mnemonic** OFFSET  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:0 | Offset     | Use to manually set the black level. See section 8.3 for more information. |

**Register Name** Gain Color Map Register  
**Address** 4A Hex  
**Mnemonic** CFAMAP  
**Type** Read/Write  
**Reset Value** 1B Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:6 | ColorMap0  | Use to program the color map for gain channel 0. See section 6.2 for more information. <b>NOTE: For monochrome sensor set all register bits[7:0] to 0.</b> |
| 5:4 | ColorMap1  | Use to program the color map for gain channel 1. See section 6.2 for more information.   |
| 3:2 | ColorMap2  | Use to program the color map for gain channel 2. See section 6.2 for more information.   |
| 1:0 | ColorMap3  | Use to program the color map for gain channel 3. See section 6.2 for more information.   |



### Register Set (continued)

**Register Name** VSYNC Latency Register  
**Address** 50 Hex  
**Mnemonic** VSYNCADJUST  
**Type** Read/Write  
**Reset Value** 08 Hex.

| Bit   | Bit Symbol                 | Description   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
|-------|----------------------------|---|-------|----------|-------|--|----|--|-------|--|-------|----------------------------|-------|----------------------|----|----|-------|------------------------|
| 7:6   |                            | Reserved.   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 4:0   | VsyncEnd                   | <p>By default, in pulse mode the <b>vsync</b> signal will remain active for four <b>pclk</b> periods after end of frame. In level mode <b>vsync</b> will remain active for the duration of the frame delay time.</p> <p>Use to adjust the time that the <b>vsync</b> signal goes inactive in multiples of <b>pclk</b> as follows:</p> <table border="1"> <tr> <td>00000</td> <td>Reserved</td> </tr> <tr> <td>00001</td> <td></td> </tr> <tr> <td>to</td> <td></td> </tr> <tr> <td>00111</td> <td></td> </tr> <tr> <td>01000</td> <td>no adjustment, the default</td> </tr> <tr> <td>01001</td> <td>+1 <b>pclk</b> clock</td> </tr> <tr> <td>to</td> <td>to</td> </tr> <tr> <td>11111</td> <td>+24 <b>pclk</b> clocks</td> </tr> </table> | 00000 | Reserved | 00001 |  | to |  | 00111 |  | 01000 | no adjustment, the default | 01001 | +1 <b>pclk</b> clock | to | to | 11111 | +24 <b>pclk</b> clocks |
| 00000 | Reserved                   |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 00001 |                            |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| to    |                            |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 00111 |                            |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 01000 | no adjustment, the default |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 01001 | +1 <b>pclk</b> clock       |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| to    | to                         |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |
| 11111 | +24 <b>pclk</b> clocks     |   |       |          |       |  |    |  |       |  |       |                            |       |                      |    |    |       |                        |

**Register Name** HSYNC Latency Register  
**Address** 51 Hex  
**Mnemonic** HSYNCADJUST  
**Type** Read/Write  
**Reset Value** 08 Hex.

| Bit   | Bit Symbol                 | Description  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
|-------|----------------------------|--|------|----------|------|--|----|--|------|--|-------|----------------------------|------|----------------------|----|----|------|-----------------------|
| 7:4   |                            | Reserved.  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 3:0   | HsyncEnd                   | <p>By default, in pulse mode the <b>hsync</b> signal will remain active for four <b>pclk</b> periods after end of each row. In level mode <b>hsync</b> will remain active for the duration of the row delay time.</p> <p>Use to adjust the time that the <b>hsync</b> signal goes inactive in multiples of <b>pclk</b> as follows:</p> <table border="1"> <tr> <td>0000</td> <td>Reserved</td> </tr> <tr> <td>0001</td> <td></td> </tr> <tr> <td>to</td> <td></td> </tr> <tr> <td>0111</td> <td></td> </tr> <tr> <td>01000</td> <td>no adjustment, the default</td> </tr> <tr> <td>1001</td> <td>+1 <b>pclk</b> clock</td> </tr> <tr> <td>to</td> <td>to</td> </tr> <tr> <td>1111</td> <td>+8 <b>pclk</b> clocks</td> </tr> </table> | 0000 | Reserved | 0001 |  | to |  | 0111 |  | 01000 | no adjustment, the default | 1001 | +1 <b>pclk</b> clock | to | to | 1111 | +8 <b>pclk</b> clocks |
| 0000  | Reserved                   |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 0001  |                            |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| to    |                            |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 0111  |                            |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 01000 | no adjustment, the default |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 1001  | +1 <b>pclk</b> clock       |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| to    | to                         |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |
| 1111  | +8 <b>pclk</b> clocks      |  |      |          |      |  |    |  |      |  |       |                            |      |                      |    |    |      |                       |

**Register Name** Synchronization Adjustment Register  
**Address** 52 Hex  
**Mnemonic** DVBUSCONFIG0  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit  | Bit Symbol            | Description   |      |                      |    |    |      |                       |
|------|-----------------------|---|------|----------------------|----|----|------|-----------------------|
| 7:4  | VsyncStart            | <p>By default, in pulse mode the <b>vsync</b> signal will remain active for four <b>pclk</b> periods after end of frame. In level mode <b>vsync</b> will remain active for the duration of the frame delay time.</p> <p>Use to adjust the time that the <b>vsync</b> signal goes active in multiples of <b>pclk</b> as follows:</p> <table border="1"> <tr> <td>0000</td> <td>0 <b>pclk</b> clocks</td> </tr> <tr> <td>to</td> <td>to</td> </tr> <tr> <td>1111</td> <td>-15 <b>pclk</b> clock</td> </tr> </table> | 0000 | 0 <b>pclk</b> clocks | to | to | 1111 | -15 <b>pclk</b> clock |
| 0000 | 0 <b>pclk</b> clocks  |   |      |                      |    |    |      |                       |
| to   | to                    |   |      |                      |    |    |      |                       |
| 1111 | -15 <b>pclk</b> clock |   |      |                      |    |    |      |                       |
| 3:0  | HsyncStart            | <p>By default, in pulse mode the <b>hsync</b> signal will remain active for four <b>pclk</b> periods after end of row. In level mode <b>hsync</b> will remain active for the duration of the row delay time.</p> <p>Use to adjust the time that the <b>hsync</b> signal goes active in multiples of <b>pclk</b> as follows:</p> <table border="1"> <tr> <td>0000</td> <td>0 <b>pclk</b> clocks</td> </tr> <tr> <td>to</td> <td>to</td> </tr> <tr> <td>1111</td> <td>-15 <b>pclk</b> clock</td> </tr> </table>     | 0000 | 0 <b>pclk</b> clocks | to | to | 1111 | -15 <b>pclk</b> clock |
| 0000 | 0 <b>pclk</b> clocks  |   |      |                      |    |    |      |                       |
| to   | to                    |   |      |                      |    |    |      |                       |
| 1111 | -15 <b>pclk</b> clock |   |      |                      |    |    |      |                       |

### Register Set (continued)

**Register Name** Polarity Adjustment Register  
**Address** 53 Hex  
**Mnemonic** DVBUSCONFIG1  
**Type** Read/Write  
**Reset Value** 0C Hex.

| Bit | Bit Symbol  | Description  |
|-----|-------------|--|
| 7   |             | Reserved   |
| 6   | PixClkMode  | Set the to a logic 1 to operate <b>pclk</b> to "data ready mode". Set to a logic 0, the default, to set <b>pclk</b> to "free running mode".  |
| 5   | VsyncMode   | Set to a logic 1 to operate the <b>vsync</b> pin to "pulse mode". Set to a logic 0, (the default) to operate the <b>vsync</b> signal to "level mode".  |
| 4   | HsyncMode   | Set to a logic 1 to operate the <b>hsync</b> signal to pulse for a minimum of four pixel clocks at the end of each row. Set to a logic 0, (the default) to force the <b>hsync</b> signal to a level indicating valid data within a row.  |
| 3   | ExtSyncPol  | Set to a logic 1, (the default), to set the active level of the <b>extsync</b> signal high. Set to a logic 0 to set the active level of the <b>extsync</b> signal low.   |
| 2   | SnapShotPol | Set to a logic 1 to set the snapshot pin to be active on the positive edge. Set to a logic 0, (the default) to set the snapshot pin to be active on the negative edge.   |
| 1   | VsyncPol    | Assert to force the <b>vsync</b> signal to generate a logic 1 during a frame readout ( <i>Level Mode</i> ), or a negative pulse at the end of a frame readout ( <i>Pulse Mode</i> ). Clear (the default) to force the <b>vsync</b> signal to generate a logic 0 during a frame readout ( <i>Level Mode</i> ), or a positive pulse at the end of a frame readout ( <i>Pulse Mode</i> ). |
| 0   | HsyncPol    | Assert to force the <b>hsync</b> signal to generate a logic 1 during a row readout ( <i>Level Mode</i> ), or a negative pulse at the end of a row readout ( <i>Pulse Mode</i> ). Clear (the default) to force the <b>hsync</b> signal to generate a logic 0 during a row readout ( <i>Level Mode</i> ), or a positive pulse at the end of a readout ( <i>Pulse Mode</i> ).             |

**Register Name** Video Output Adjustment Register  
**Address** 54 Hex  
**Mnemonic** DVBUSCONFIG2  
**Type** Read/Write  
**Reset Value** F0 Hex.

| Bit  | Bit Symbol                 | Description  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
|------|----------------------------|--|------|--------------------|------|-------------------------|------|---------------------------|------|----------------------------|------|----------------------------|------|---------------------------|------|----------------------------|------|----------------------------|------|---------------------------|------|--------------------------|------|---------------------|
| 7    | OutputEn                   | Set to a logic 0 to tri-state all output signals (data and control) on the digital video port. set to a logic 1, (the default) to enable all signals (data and control) on the digital video port.   |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 6    | BlkPixelEn                 | Set to a logic 1, (the default) to read out the middle 8 black pixels at the start of every row. Set to a logic 0 to mask out the black pixel readout.   |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 5    | PixClkPol                  | Set to a logic 1 to set the active edge of the pixel clock to negative. Set to a logic 0, (the default), to set the active edge of the clock to positive.  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 4    |                            | Reserved   |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 3:0  | Bshift[3:0]                | Use to program the routing of the MSB output of the internal video A/D to a bit on the digital video bus.<br><br><table border="1"> <tr><td>0000</td><td>A/D[9:0] -&gt; d[9:0]</td></tr> <tr><td>0001</td><td>A/D[9:0] -&gt; d[8:0],d[9]</td></tr> <tr><td>0010</td><td>A/D [9:0] -&gt;d[7:0],d[9:8]</td></tr> <tr><td>0011</td><td>A/D [9:0] -&gt; d[6:0],d[9:7]</td></tr> <tr><td>0100</td><td>A/D [9:0] -&gt; d[5:0],d[9:6]</td></tr> <tr><td>0101</td><td>A/D[9:0] -&gt; d[4:0],d[9:5]</td></tr> <tr><td>0110</td><td>A/D [9:0] -&gt; d[3:0],d[9:4]</td></tr> <tr><td>0111</td><td>A/D [9:0] -&gt; d[2:0],d[9:3]</td></tr> <tr><td>1000</td><td>A/D [9:0] -&gt;d[1:0],d[9:2]</td></tr> <tr><td>1001</td><td>A/D [9:0] -&gt; d[0],d[9:1]</td></tr> <tr><td>1010</td><td>A/D [9:0] -&gt; d[9:0]</td></tr> </table> | 0000 | A/D[9:0] -> d[9:0] | 0001 | A/D[9:0] -> d[8:0],d[9] | 0010 | A/D [9:0] ->d[7:0],d[9:8] | 0011 | A/D [9:0] -> d[6:0],d[9:7] | 0100 | A/D [9:0] -> d[5:0],d[9:6] | 0101 | A/D[9:0] -> d[4:0],d[9:5] | 0110 | A/D [9:0] -> d[3:0],d[9:4] | 0111 | A/D [9:0] -> d[2:0],d[9:3] | 1000 | A/D [9:0] ->d[1:0],d[9:2] | 1001 | A/D [9:0] -> d[0],d[9:1] | 1010 | A/D [9:0] -> d[9:0] |
| 0000 | A/D[9:0] -> d[9:0]         |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0001 | A/D[9:0] -> d[8:0],d[9]    |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0010 | A/D [9:0] ->d[7:0],d[9:8]  |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0011 | A/D [9:0] -> d[6:0],d[9:7] |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0100 | A/D [9:0] -> d[5:0],d[9:6] |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0101 | A/D[9:0] -> d[4:0],d[9:5]  |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0110 | A/D [9:0] -> d[3:0],d[9:4] |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 0111 | A/D [9:0] -> d[2:0],d[9:3] |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 1000 | A/D [9:0] ->d[1:0],d[9:2]  |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 1001 | A/D [9:0] -> d[0],d[9:1]   |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |
| 1010 | A/D [9:0] -> d[9:0]        |  |      |                    |      |                         |      |                           |      |                            |      |                            |      |                           |      |                            |      |                            |      |                           |      |                          |      |                     |

### Register Set (continued)

**Register Name** Video Output Tristate Adjustment Register  
**Address** 55 Hex  
**Mnemonic** DVBUSCONFIG3  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol      | Description   |
|-----|-----------------|---|
| 7:5 |                 | Reserved  |
| 4   | Tristate        | Digital output tristate. Set this bit to 1 to tristate all digital outputs. ( <b>vsync</b> , <b>hsync</b> , <b>pclk</b> , <b>data</b> , external sync). Use can override this setting with independent override bits. |
| 3   | VsOverride      | Overrides tri-stating of Vsync port in master timing mode. To enable override, set bit to 1.  |
| 2   | HsOverride      | Overrides tri-stating of Hsync port in master timing mode. To enable override, set bit to 1.  |
| 1   | PclkOverride    | Overrides tri-stating of Pclk port in master timing mode. To enable override, set bit to 1.   |
| 0   | ExtSyncOverride | Overrides tri-stating of external sync port in master timing mode. To enable override, set bit to 1.  |

**Register Name** Initialization Register 1  
**Address** 80 Hex  
**Mnemonic** INTREG1  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description   |
|-----|------------|---|
| 7:0 | PixCal     | Write 5 Hex to enable the pixel offset calibration circuits.<br><br>Notes:<br><br>This register can only be accessed when the Int2 parameter in the INTREG2 register is set to 01Hex.<br><br>PixCal should be reset to 00Hex at the end of the pixel offset calibration procedure (see section 8.1 for more details). |

**Register Name** Pixel Offset Register  
**Address** 83 Hex  
**Mnemonic** PIXELOFFSET  
**Type** Read/Write  
**Reset Value** 1E Hex.

| Bit | Bit Symbol  | Description   |
|-----|-------------|---|
| 7:0 | PixelOffset | Use to compensate for the sensors natural pixel offset. See section 8.1 for more details. |

**Register Name** Power Down Control Register  
**Address** 85 Hex  
**Mnemonic** POWCTRL  
**Type** Read/Write  
**Reset Value** 81 Hex.

| Bit | Bit Symbol | Description   |
|-----|------------|---|
| 7:0 | Patrol     | Write 82Hex before power down to minimize the sensor's power down current.<br><br>Write 86Hex after power up from the power down mode to ensure correct operation of the sensor. This puts sensor in bandgap mode, where the references are generated by an internal bandgap.<br><br>Write 81Hex after power up to set the part<br><br>Refer to section 9.2 for more information. |

**Register Name** Initialization Register 2  
**Address** 88 Hex  
**Mnemonic** INTREG2  
**Type** Read/Write  
**Reset Value** 00 Hex.

| Bit | Bit Symbol | Description  |
|-----|------------|--|
| 7:0 | Int2       | Write 1 Hex to activate the sensor's initialization registers<br><br>Write 0 Hex to disable the sensor's initialization registers.<br><br>Note this register is used for<br><ul style="list-style-type: none"> <li>the pixel array offset calibration (section 8.2)</li> <li>power/up and down of the array (section 9.2)</li> </ul> |

## Timing Information

### 1.0 DIGITAL VIDEO PORT MASTER MODE TIMING

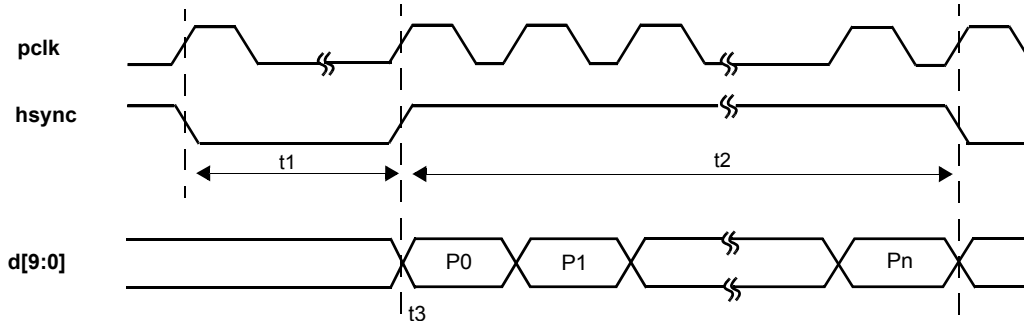


Figure 53. Row Timing Diagram

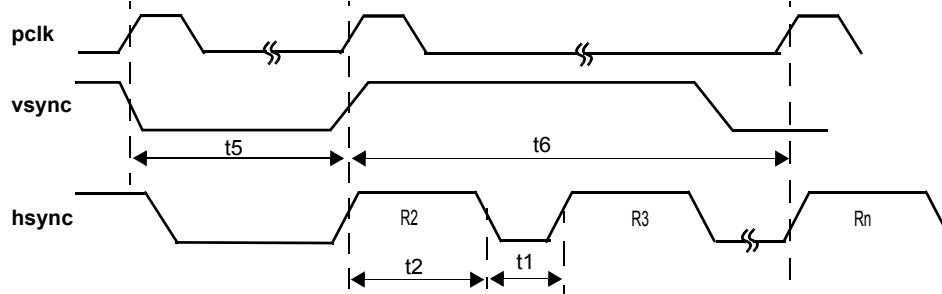


Figure 54. Frame Timing

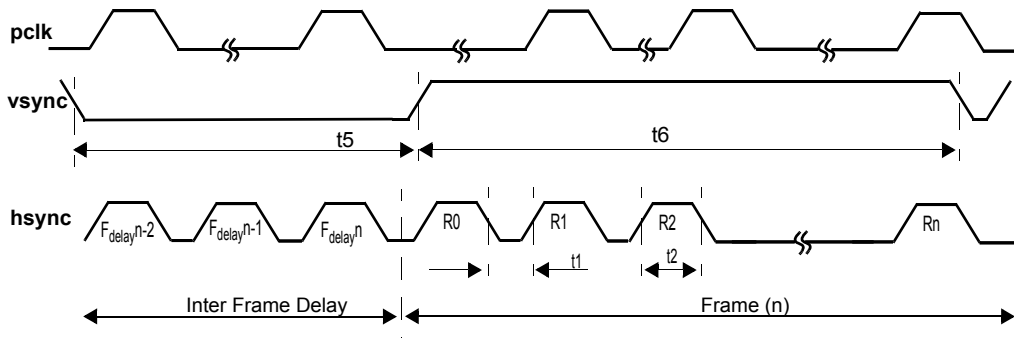


Figure 55. Frame Delay Timing (With Inter Frame Delay).

| Label | Descriptions   | Min                      | Typ  | Max     |
|-------|--|--------------------------|--|---------|
| t0    | pclk period  | 83.33ns                  | 45.45ns  | 37.04ns |
| t1    | hsync inactive <sup>1,2</sup>                          | level mode<br>pulse mode | $(RN_{Hclk} - N_{pix} + HsyncStart - HsyncEnd) * Hclk$<br>$(RN_{Hclk} - 4) * Hclk$                             |         |
| t2    | hsync active <sup>1,2</sup>                            | level mode<br>pulse mode | $(HsyncEnd - HsyncStart + N_{pix}) * Hclk$<br>$4 * Hclk$   |         |
| t3    | first valid pixel data after hsync active <sup>4</sup> |                          | $t_{hstart} * Hclk$  |         |
| t5    | vsync inactive <sup>1,3</sup>                          | level mode<br>pulse mode | $(F_{delay} * RN_{Hclk} + R_{opcycle} + R_{itime} + VsyncStart - VsyncEnd) * Hclk$<br>$(FN_{Hclk} - 4) * Hclk$ |         |
| t6    | vsync active <sup>1,3</sup>                            | level mode<br>pulse mode | $((VsyncEnd - VsyncStart) + (RN_{Hclk} * N_{rows})) * Hclk$<br>$4 * Hclk$                                      |         |

Note 1: 1. See section 6.4 for definitions of  $RN_{Hclk}$ ,  $N_{pix}$  and  $FN_{Hclk}$   
 Note 2: 2. The values of  $HsyncStart$  and  $HsyncEnd$  are stored in the  $DVBUSCONFIG0$  and  $HSYNCADJUST$  registers respectively.  
 Note 3: 3. The values of  $VsyncStart$  and  $VsyncEnd$  are stored in the  $DVBUSCONFIG0$  and  $VSYNCADJUST$  registers respectively.  
 Note 4: 4. See register  $DVBUSCONFIG0$  to set  $t_{hstart}$  ( $HsyncStart$ ). These bits can move the start of  $Hsync$  up to 15  $Pclk$ 's before valid data is available.

Timing Information (continued)

2.0 DIGITAL VIDEO PORT SLAVE MODE TIMING

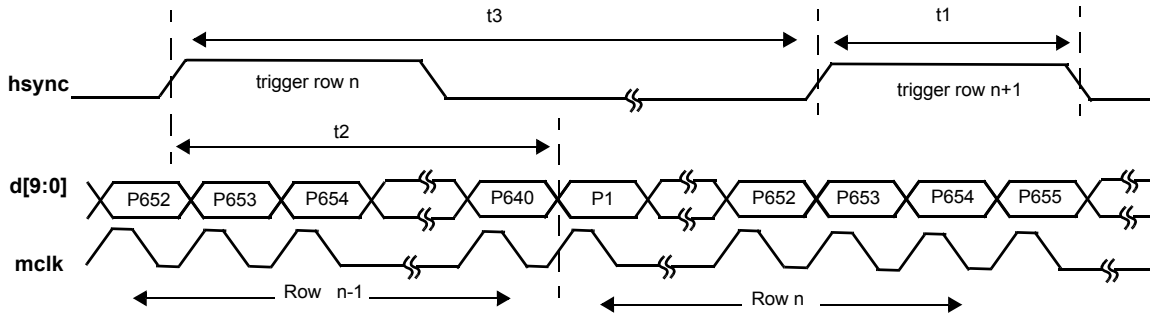


Figure 56. Slave Mode Row Trigger and Readout Timing

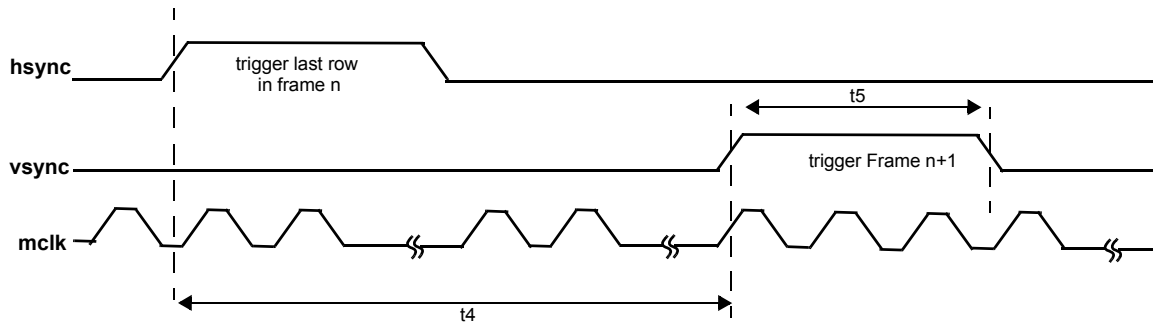


Figure 57. Slave Mode d[9:0], hsync & vsync to pclk Timing

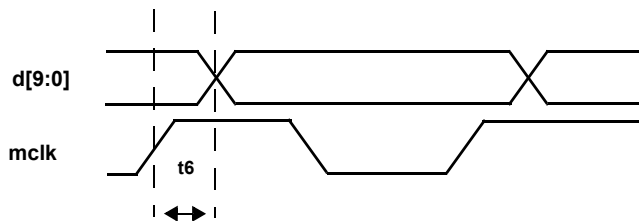


Figure 58. Rising Edge of mclk to Valid Pixel Data

| Label | Descriptions   | Min                       | Typ               | Max |
|-------|--|---------------------------|-------------------|-----|
| t1    | Pulse width of row trigger   | 2 * mclk                  |                   |     |
| t2    | First pixel out after rising edge of row trigger <sup>1</sup>              |                           | X <sub>pclk</sub> |     |
| t3    | Minimum time between row triggers <sup>2</sup>                             | RN <sub>Hclk</sub> * Hclk |                   |     |
| t4    | Time to assert next frame trigger after last row trigger in current frame. | 20 * Hclk                 |                   |     |
| t5    | Pulse width of Frame trigger   | 2 * mclk                  |                   |     |
| t6    | Time to valid pixel data after rising edge of mclk                         |                           | 44ns              |     |

1. See section 11.7 for definition of X<sub>pclk</sub>

2. See section 6.4 for definition of RN<sub>Hclk</sub>

Timing Information (continued)

3.0 DIGITAL VIDEO PORT SINGLE FRAME CAPTURE (SNAPSHOT MODE) TIMING

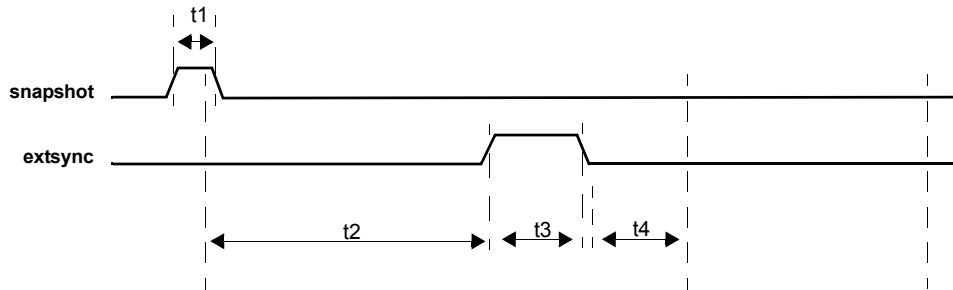


Figure 59. Snapshot Mode Timing With External Shutter

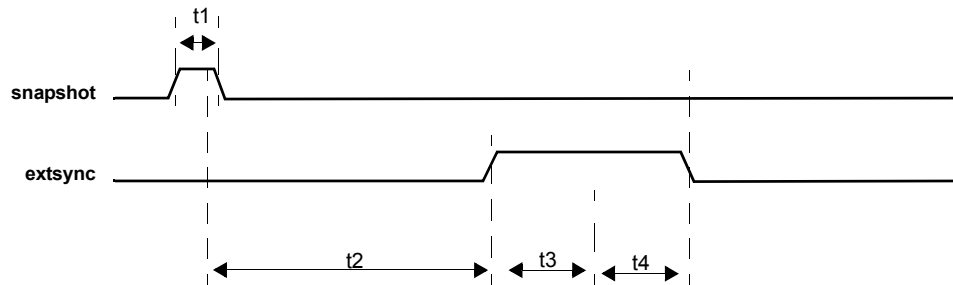


Figure 60. Snapshot Timing Without External Shutter

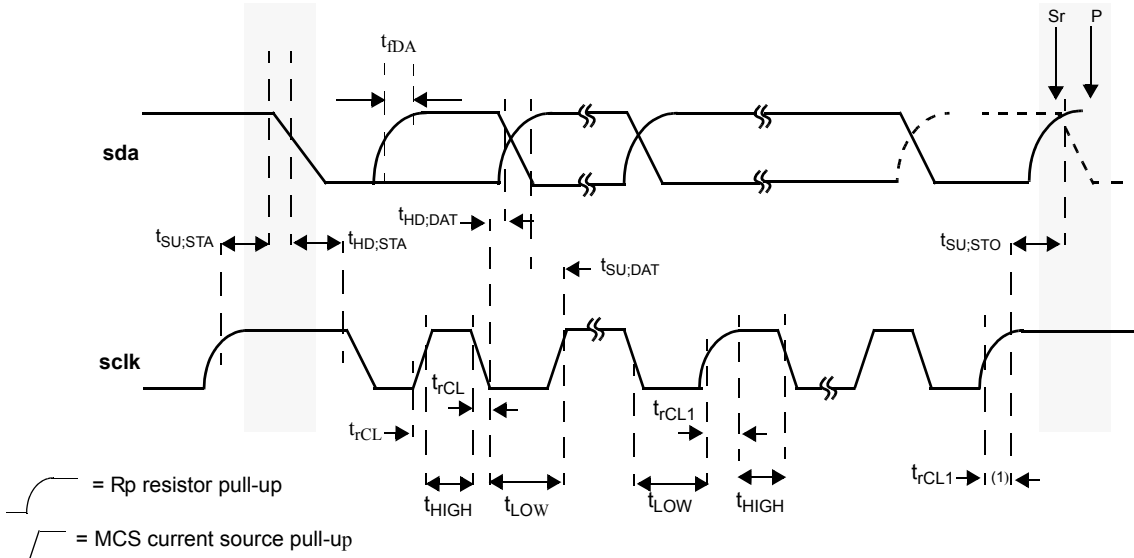
| Label | Descriptions                                       | Equation                         |
|-------|--|----------------------------------|
| t1    | Minimum Snapshot Trigger Pulse Width               | $2 \cdot mclk$ (see notes a & b) |
| t2    | Minimum time from Snapshot Pulse to <b>extsync</b> | $FN_{Hclk}$ (see notes a & b)    |
| t3    | Array Integration Time                             | $FN_{Hclk}$ (see notes a & b)    |
| t4    | Pixel Read Out                                     | $FN_{Hclk}$ (see notes a & b)    |

Note a: See *Frame Rate Programming* section for more details

Note b: See *Snapshot Mode* for more details

**Timing Information** (continued)

**4.0 SERIAL BUS TIMING**



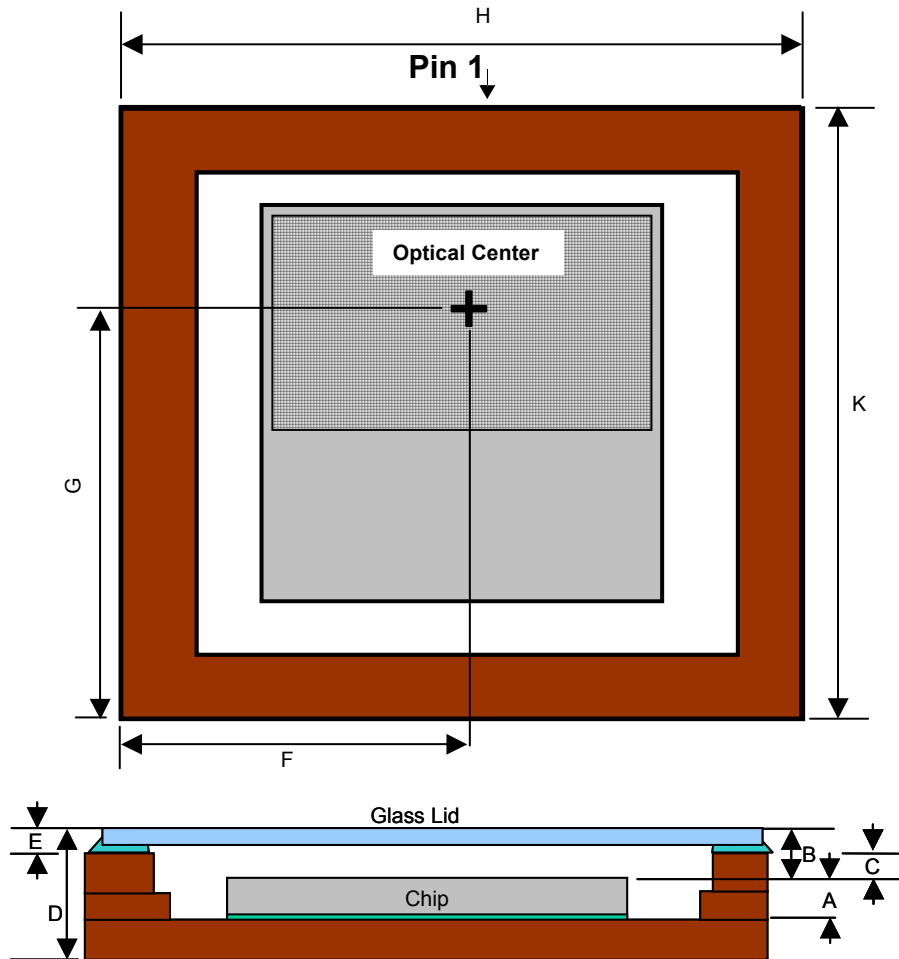
(1) Rising edge of the first **sclk** pulse after an acknowledge bit.

**Figure 61. I<sup>2</sup>C Compatible Serial Bus Timing.**

The following specifications apply for all supply pins = +3.3V, C<sub>L</sub> = 10pF, and **sclk** = 400KHz unless otherwise noted. **Boldface limits apply for TA = T<sub>MIN</sub> to T<sub>MAX</sub>**; all other limits TA = 25°C (Note 7)

| PARAMETER                                 | SYMBOL                  | MIN | MAX | UNIT |
|---|-------------------------|-----|-----|------|
| <b>sclk</b> clock frequency               | <b>f<sub>SCLH</sub></b> | 0   | 400 | KHz  |
| Set-up time (repeated) START condition    | t <sub>SU:STA</sub>     | 0.6 | -   | μS   |
| Hold time (repeated) START condition      | t <sub>HD:STA</sub>     | 0.6 | -   | μS   |
| LOW period of the <b>sclk</b> clock       | t <sub>LOW</sub>        | 1.3 | -   | μS   |
| HIGH period of the <b>sclk</b> clock      | t <sub>HIGH</sub>       | 0.6 | -   | μS   |
| Data set-up time                          | t <sub>SU:DAT</sub>     | 180 | -   | nS   |
| Data hold time                            | t <sub>HD:DAT</sub>     | 0   | 0.9 | μS   |
| Set-up time for STOP condition            | t <sub>SU:STO</sub>     | 0.6 | -   | μS   |
| Capacitive load for and <b>sclk</b> lines | C <sub>b</sub>          | -   | 400 | pF   |

**Mechanical Information**



| Dimension | Description                                       | min (mm) | typ (mm) | max (mm) |
|-----------|---|----------|----------|----------|
| A         | Distance from top of chip to bottom of cavity     | 0.788    | 0.820    | 0.852    |
| B         | Top of die to top of glass lid                    | 0.690    | 0.970    | 1.250    |
| C         | Top of Package to top chip                        | 0.250    | 0.420    | 0.590    |
| D         | Max total thickness of package, glass, and epoxy. |          |          | 2.580    |
| E         | Thickness of lid and epoxy                        | 0.530    | 0.640    | 0.750    |
| F         | X-Coordinate of optical center (nom)              |          | 7.110    |          |
| G         | Y-Coordinate of optical center (nom)              |          | 8.100    |          |
| H         | X-Dimension of Package                            | 14.090   | 14.220   | 14.520   |
| K         | Y-Dimension of Package                            | 14.090   | 14.220   | 14.520   |



# Package Information

**RECOMMENDED LAND PATTERN**

| REVISIONS |                             |        |            |          |
|-----------|-----------------------------|--------|------------|----------|
| LTN       | DESCRIPTION                 | E.C.N. | DATE       | BY/APP'D |
| A         | RELEASE TO DOCUMENT CONTROL | 12126  | 12/07/1998 | MS/AP    |
| B         | ADD OPTICAL CTR & NOTE 3    | 12210  | 08/13/1999 | TL/AP    |
| C         | REMOVE OPTICAL CTR & NOTE 3 | 454    | 11/01/2001 | TL/AP    |
| D         | ADD LAND PATTERN            | 504    | 12/12/2001 | TL/AT    |

**CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS**

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL EXPOSED METALIZED AREAS SHALL BE GOLD PLATED 60 MICROINCHES (1.52 MICROMETERS) MINIMUM THICK OVER NICKEL PLATE.
- REFERENCE JEDEC REGISTRATION MS-009, VARIATION AF.

| APPROVALS              |  | DATE       |
|------------------------|--|------------|
| DRWN: MARTA SUCHY      |  | 12/07/1998 |
| DFTG. CHG: MARTA SUCHY |  | 12/12/2001 |
| ENGR. CHG: ANNY TU     |  | 12/12/2001 |

**LEADLESS CHIP CARRIER,  
CERAMIC, .560x.560x.102in,  
48 TERMINAL, .040in PITCH**

|            |       |      |                |     |
|------------|-------|------|----------------|-----|
| PROJECTION | SCALE | SIZE | DRAWING NUMBER | REV |
|            | N/A   | C    | (SC)MKT-EA48A  | D   |

DO NOT SCALE DRAWING      SHEET 1 of 1

\*Refer to Mechanical Information on Page 40 for information on optical center

## Revision Changes

| Revision Number | Description  |
|-----------------|--|
| 1.94            | <p>Page 3 - moved figure 1 text so it was outside of diagram</p> <p>Page 3 - changed ordering information as follows: Changed package field to part number, added Kodak part numbers, added lens kit information.</p> <p>Page 5 - Added text stating SDA and SCLK were open drain I/O's</p> <p>Page 6 - Changed Pin 45 from Pwn to Pwd to match rest of datasheet</p> <p>Page 9 - Under Blemish Specification changed National Semiconductor to Eastman Kodak</p> <p>Page 13 and 14 - changed all references to 2:1 subsampling to sub-sampling</p> <p>Page 14 - Section 5.4 changed all references to 2:1 sub-sampling to 4:2 sub-sampling</p> <p>Page 14 - updated figure references to refer to proper figure</p> <p>Page 16 - Section 6.3 in section defining Hclk changed Mclk can be divided by 2,4, or 6 to say Mclk can be divided by 1 or 2.</p> <p>Page 17 - Section 6.4 corrected all references to WEndCol as end column and WStartCol as start column</p> <p>Page 17 - Section 6.4 corrected all references to WEndRow as end row and WStartRow as start row.</p> <p>Page 17 - Section 6.4 changed Fdelays maximum programmable value from 32766 to 32767</p> <p>Page 15 - under figure 14 after the following words "The following factors effect exposure and signal level" changed integration time to programmed partial frame integration.</p> <p>Page 18 - Section 7.3 changed max external trigger pulse from 32768 to 32767</p> <p>Page 18 - Section 7.3 changed array reset from 0-8 frames to 1-8 frames.</p> <p>Page 19 - Section 9.2 changed pwn pin to pwd pin.</p> <p>Page 19 - Section 9.2 removed bandgap references and replaced with internal reference ladder.</p> <p>Page 20 - Section 10.0 added that Mclk must be running and 4x faster than Sclk for I2C to work.</p> <p>Page 21 - Section 11.2 added section title to Synchronisation Signals ...</p> <p>Page 24 - added section heading for Slave Mode</p> <p>Page 24 - added arrow to Pclk in Figure 51</p> <p>Page 25 and 27 - Register 0x09h OPCTRL - changed reset value from 0x02h to 0x06h</p> <p>Page 25 and 27 - Register 0x01h REV - changed reset value from Latest Silicon to 0x09h</p> <p>Page 27 - Register 0x05h VCLKGEN - changed bit 2 to reserved. Can only divide Mclk by a maximum of 2</p> <p>Page 29 - Register 0x1Bh - changed bits 1:0 of both WStartRow and WEndRow to be reserved.</p> <p>Page 29 - Register 0x1Eh - changed bits 1:0 of both WStartCol and WEndCol to be reserved.</p> <p>Page 40 - updated descriptions so they matched drawing.</p> <p>All Pages - removed part number from side of page and added part number to bottom of page.<br/>Added Revision history to datasheet.</p> |